Considerations for High-Speed Configurable-bandwidth Time-interleaved Digital Delta-Sigma Modulators and Synthesis in 28 nm UTBB FDSOI

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***Abstract*—This paper presents the design and simulation of a time-interleaved delta-sigma modulator as part of a digital transmitter chain. The architecture is chosen based on a critical path analysis in order to reach very high frequency operation. The modulator's configurability allows it to target signal bandwidths from 20 MHz up to 160 MHz with a SNR greater than 67 dB. Finally, the modulator is synthesized using standard cells in 28nm FDSOI CMOS from STMicroelectronics and simulated for different numbers of time-interleaved channels, reaching a sample rate of up to 6 GS/s. An optimum number of channels can be found based on a trade-off between operating frequency, supply voltage, power consumption and area.**

Keywords— Delta Sigma Modulator (DSM), time-interleaving, critical path analysis, digital transmitter;

I. INTRODUCTION

The high demand of more and more performant mobile communication systems has determined a shift from analog to digital processing in transmitter architectures (Fig. 1), in order to overcome associated challenges, such as high data rates, configurability for multi-standard, area and power consumption reduction [1-2].

Furthermore, [3] introduces an all-digital signal generator based on single-bit error-feedback delta-sigma modulator (DSM) directly at RF frequencies, targeting UMTS standard. The advantages of this implementation are the 1-bit output which ensures high linearity and high efficiency of the succeeding power amplifier (PA) stage and the simplification of the mixer stage which allows a reduced working frequency for the DSM, namely twice the carrier frequency f_c instead of 4 times f_c. In order to be able to target more performant communication standards and to reduce the in-band quantization noise, the sampling frequency of the modulator should be increased. However, this would also mean increased timing constraints which are hard to meet in a traditional DSM.

A solution is to introduce time-interleaved (TI) operation, thus relaxing the timing constraints of the system [4-7]. A 2nd order multi-stage noise shaping (MASH) architecture with 8 TI channels is presented to work at an effective sampling frequency of 2.5 GHz while consuming 6.9 mW [4]. An extended study of the critical path for a similar architecture is performed in [5] in order to increase the sampling frequency up to 8 GHz, though the power consumption is 10 times larger than in [4].

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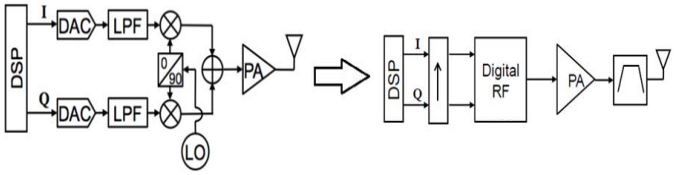

Fig. 1. Traditional Transmitter (left); Digital Transmitter (right)

Nevertheless, the MASH architecture has a multi-bit output which requires the use of an additional Digital-to-Analog Converter (DAC) and doesn't allow bandwidth configurability, since all the zeros of the noise shaping function are located at DC. Hence, error feedback DSMs have been preferred and will be studied further.

This paper details the step-by-step design of a DSM, which has been synthesized for high-speed applications up to 6 GHz sampling frequency and signal bandwidths from 20 MHz up to 160 MHz with a SNR greater than 67 dB. Therefore, it is shown that the main advantage of time-interleaving is the possibility to increase the effective sampling frequency thanks to the relaxed timing constraints.

The remainder of this paper is organized as follows. Section II presents the critical path analysis of known error feedback DSM architectures using time-interleaving. Section III introduces the proposed implementation with added configurability for improved SNR performances. Section IV presents the synthesis and simulations of the designed modulator. Finally, conclusions are presented in Section V.

II. TIME INTERLEAVING IN ERROR-FEEDBACK DSM

A. 1st order DSM

The diagram of a 1st order DSM incorporating a single-bit quantizer along with a discrete-time integrator in negative feed-back is displayed in Fig. 2. The output in z-domain is given by

$$Y(z) = X(z)\cdot z^{-1} + E(z)\cdot(1-z^{-1}) \quad (1)$$

where $X(z)$, $Y(z)$ and $E(z)$ are the z-transforms of the input, output and the quantization error, respectively. It can be seen that the input signal is filtered by the signal transfer function $STF(z) = z^{-1}$, while the quantization error is high-pass filtered by the noise transfer function $NTF(z) = (1-z^{-1})$. Thus, the quantization noise is pushed away from the in-band to the out-of-band in order to improve the SNR.

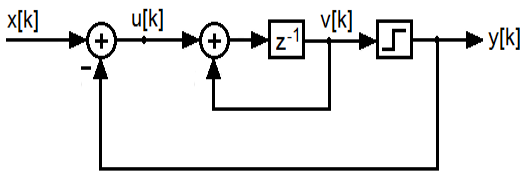

Fig. 2. 1st order DSM architecture

TABLE I. HARDWARE COMPARISON FOR L[TH]-ORDER M-CHANNEL TI DSM [7]

	Block digital filtering [6]	TI reduced complexity [7]
No. integrators	*LM*	*none*
No. cross-connections	$L(M^2-M)$	$(L+1)M$
No. delay elements	*M*	*L*
No. two-input adders	$L(M^2-M)$	*LM*

B. TI DSM methods

The architectures in [4-5] use the popular block digital filtering method for time-interleaving, introduced over 20 years ago in [6]. This method is based on poly-phase components and results in an effective sampling frequency of Mf_S, where M is the number of cross-coupled DSMs operating at the sampling frequency f_S. However, [7] has introduced a new method with reduced complexity in terms of hardware requirements which is based on the equations in each node of the modulator.

A comparison between these 2 methods is made in [7] in terms of hardware requirements for a L^{th} order M-channel DSM (Table I), showing a highly reduced complexity especially when increasing the number of channels. Nevertheless, this method has been used only recently in a 4-channel TI DSM implementation on FPGA working at a maximum sampling frequency of 400 MHz with a narrow signal bandwidth of 1.25 MHz [8].

C. Critical path analysis

The architectures of a 1st order 2-channel DSM using the poly-phase and node equations methods are displayed in Fig. 3. Assuming that the addition between 2 n-bit signals introduces a delay proportional to n and an addition between a n-bit signal and a d_a -bit signal ($d_a <= n$) introduces a reduced delay, we can estimate the delay factor of the critical path for the two methods.

Therefore, in the case of a 1st-order 2-channel modulator, a delay factor of $D_{pf} = 4n + 2d_a$ is obtained for the poly-phase method and $D_{neq} = 2n + 2d_a$ for the node equations method, respectively. The value d_a depends on the value of the coefficient a.

Thus, if $a = 2^0$, the summation will involve only the most significant bit (MSB) and in this case $d_a = 1$, whereas in the worst case, when $a = 2^{-n+1}$, the summation is performed on all n bits, hence $d_a = n$. This means that $D_{neq} \approx (1/2) \cdot D_{pf}$ in the best case ($d_a = 1$) and $D_{neq} = (2/3) \cdot D_{pf}$ in the worst case ($d_a = n$). Consequently, the node equations method is more suited for high-speed applications, since it employs less hardware with relaxed timing constraints.

Next, the node equations method has been applied for different number of channels to known architectures of error-feedback DSMs, such as Cascade-of-integrators feedback form (CIFB) [3], Cascade-of-integrators feedforward form (CIFF) [9], Cascade-of-resonators feedback form (CRFB) [10], Cascade-of-resonators feedforward form (CRFF) [11].

The critical path of the 4 architectures for 2nd order with 2 channels is analyzed and estimated in Table II. It can be seen that the critical path of the CIFB architecture is almost half of the next best one, CIFF and almost a third of the poly-phase CRFB implementation in [10]. Hence, the study has been extended in Table III to a 3rd order CIFB architecture with up to 8 channels time-interleaving.

The impact of optimizing zeros placement (not at DC), in order to target larger bandwidth signals, is also taken into account in this table. Thus, a trade-off has to be made between the signal bandwidth and the effective sampling frequency, since the architecture with zero placement optimization has a 50% larger critical path delay than the one of the architecture with all zeros at DC.

In addition, it is shown that increasing the modulator order in the case of the CIFB architecture doesn't affect the critical path length. This has been highlighted in Table II and III for 2nd and 3rd order, respectively. This study also indicates that doubling the number of channels determines an increase of the delay in the critical path by a factor of 2, except from 1 to 2 channels where the factor is about 1.5. Nevertheless, optimizations in the digital synthesis flow can be more efficient on long critical paths and highly-interleaved modulator can be beneficial for achieving high speed operation.

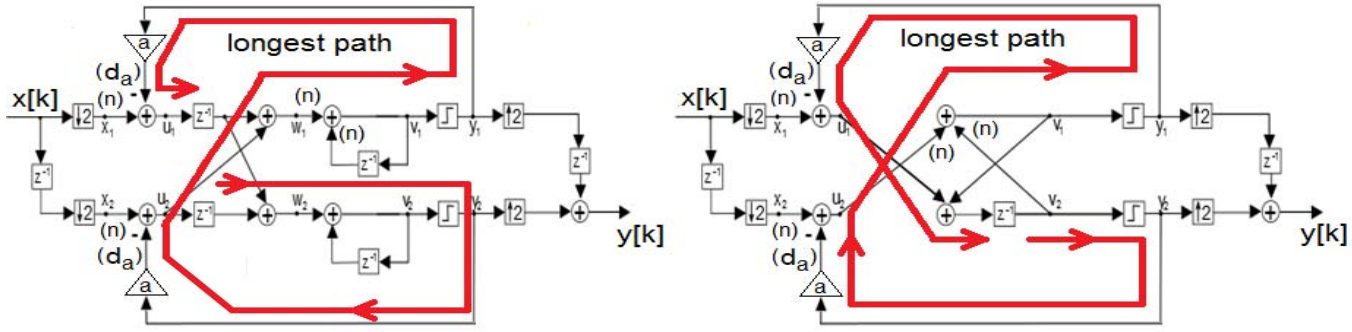

Fig. 3. 1st order 2-channel DSM architecture: poly-phase method (left); node equations (right)

TABLE II. CRITICAL PATH IN ERROR-FEEDBACK TI DSM

Architecture TI Method		Critical path	
		General	Worst case ($d_a = n$)
CIFB 2nd order 2 channels	Node equations	$\boldsymbol{3n + 2d_a}$	$5n$
CIFF 2nd order 2 channels	Node equations	$6n + 2d_a$	$8n$
CRFB 2nd order 2 channels	Node equations	$6n + 4d_a$	$10n$
CRFF 2nd order 2 channels	Node equations	$8n + 2d_a$	$10n$
CRFB 2nd order 2 channels [10]	Poly-phase	$9n + 2d_a$	$11n$

TABLE III. CRITICAL PATH IN CIFB DSM M-TI CHANNELS

Architecture	M-TI Channels	Critical path	
		Optimized zeros	Zeros at DC
CIFB 3rd order	1	$2n + 2d_a$	$n + d_a$
CIFB 3rd order	2	$\boldsymbol{3n + 2d_a}$	$2n + 2d_a$
CIFB 3rd order	4	$6n + 4d_a$	$4n + 4d_a$
CIFB 3rd order	8	$12n + 8d_a$	$8n + 8d_a$

III. CIFB ARCHITECTURE

As it has been shown in the previous section, the implementation of the coefficients influences the delay factor of the critical path which in the end determines the maximum sampling frequency of the modulator. In order to obtain simplified operations, all the coefficients have been quantized to negative powers of 2, thus avoiding dedicated multipliers. Figure 4 details the implemented coefficients of a 3rd order CIFB DSM with optimized zero placement, designed to target up to 160 MHz signal bandwidths. The d_a value is computed as the average of all coefficients, leading to $d_a \approx (1/3)\ n$.

During the design phase, it has been observed that the optimized zero placement ($g_1 \neq 0$) is suited only for signal bandwidths larger than 80 MHz. Otherwise, the placement of zeros at DC ($g_1 = 0$) gives better results in terms of peak SNR in the case of signals with smaller bandwidth. This behavior is visible in Fig. 5, where the *NTFs* of the modulator with all the zeros at DC (curve "1") and with zero placement optimization (curve "2") are plotted. Therefore, the magnitude of the *NTF* for $g_1 = 0$ is optimal for signal bandwidths of 20 MHz up to 80 MHz, whereas for the 160 MHz case, the magnitude of the *NTF* for $g_1 = 2^{-7}$ becomes optimal.

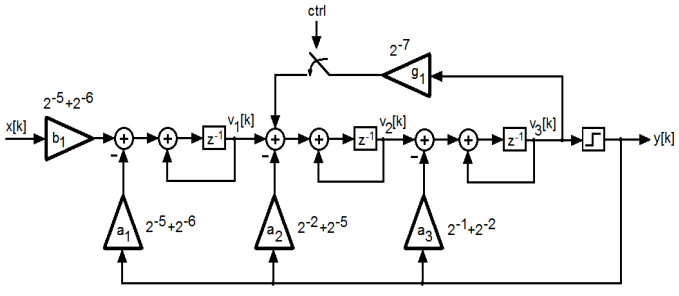

Fig. 4. 3rd order CIFB DSM architecture with added control

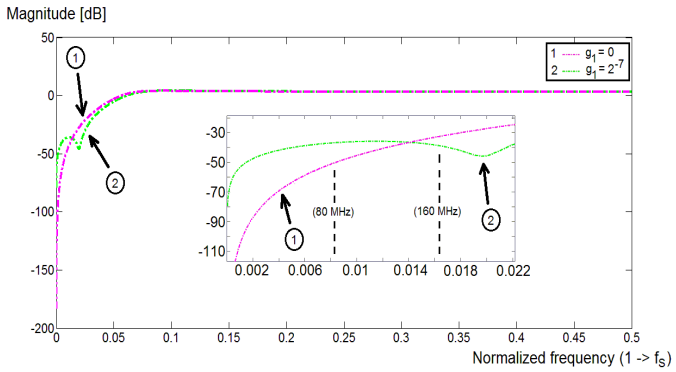

Fig. 5. *NTFs* of the 3rd order CIFB DSM: $g_1 = 0$; $g_1 = 2^{-7}$

TABLE IV. PEAK SNR 3RD ORDER CIFB DSM

BW [MHz]	OSR	Peak SNR [dB] (*ideal*)	Peak SNR [dB] (*quantized*)	Peak SNR [dB] (*optimized*)
20	240	134.1	89.9[a]	127.4[b]
40	120	112.3	78.6[a]	104[b]
80	60	91.4	71.7[a]	82.4[b]
160	30	69.2	67.2[a]	67.2[a]

a. g_1 activated
b. g_1 deactivated

Consequently, using only a 1-bit control signal (*ctrl*) to activate or deactivate the g_1 coefficient, as shown in Fig. 4, the architecture can be easily configured and optimized depending on the signal bandwidth, thus improving the SNR in different scenarios with extremely low effort.

Table IV contains the values of peak SNR for the targeted signal bandwidths (BW) and corresponding oversampling ratios (OSR). The case *ideal* corresponds to ideal coefficients, *quantized* corresponds to quantized coefficients with g_1 activated for 20-160 MHz and *optimized* corresponds to quantized coefficients with g_1 activated for 160 MHz and g_1 deactivated for 20-80 MHz, respectively. First, when comparing the *quantized* and *ideal* cases, it can be noticed that the SNR is similar for the 160 MHz case and decreases by about 44 dB for the 20 MHz case. In addition, the deactivation of the g_1 coefficient confirms it to be a valuable feature of this implementation, especially for the 20 MHz bandwidth where the SNR is improved by up to 37 dB with respect to the *quantized* case.

IV. TI DSM SYNTHESIS

The proposed CIFB DSM has been synthesized for different number of TI-channels using standard cells in 28nm FDSOI CMOS from STMicroelectronics. The results in terms of critical path slack have been obtained for a set of three supply voltages, {0.8, 0.9, 1} V. Thus, the maximum effective sampling frequency of the modulators with respect to the supply voltage can be estimated, reaching up to 6 GHz for 5 TI-channels operating at 1 V (Fig. 6). It is first noticed that the maximum frequency for 3-channels TI DSM is ~30% higher than its non-TI counterpart, which confirms the critical path study.

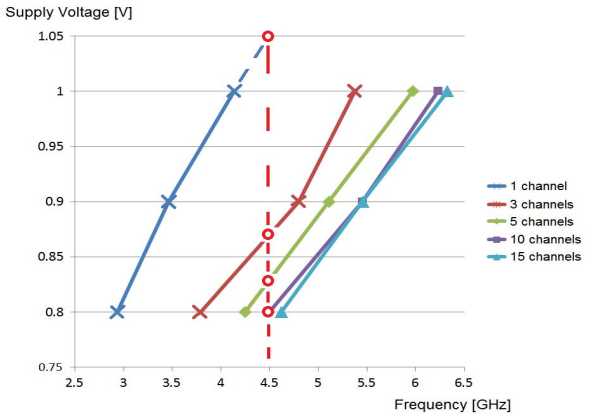

Fig. 6. TI DSM maximum effective sampling frequency vs. supply voltage

Furthermore, increasing the number of TI-channels will allow operation at increased frequency, since the optimization introduced by the synthesizer can be more efficient for longer critical paths. However, increasing the number of TI channels above 10 does not bring enhanced operating frequency while the complexity increases. Additionally, if the application requires lower operating frequency, the time-interleaved modulators can operate at a reduced supply voltage in order to improve the power consumption. For instance, in the case of a 10-channel TI DSM operating at 4.5 GHz, the supply voltage can be lowered down to 0.8 V.

The power consumption with respect to the number of TI-channels for the operating frequency of 4.5 GHz and different supply voltages is presented in Table V. It can be seen, that up to 5 channels the power consumption remains around 6-7 mW, whereas a further increase of the number of channels will lead to a much higher power consumption.

The 5-channel TI DSM synthesized with standard cells in 28nm FDSOI CMOS from STMicroelectronics occupies an 80 µm x 80 µm silicon area. It has been simulated for an input sinewave at 5 MHz, reaching an effective sampling frequency of 6 GHz with a power consumption of 11.4 mW at a 1 V supply voltage (Fig. 7). These results show an improvement in the maximum sampling frequency with a factor of 2 to 3 with respect to the non-TI CIFB DSM [3] and 8-channel TI MASH [4]. In comparison with the 2-channel TI MASH [5], the proposed architecture doesn't require the use of an additional DAC, allows bandwidth configurability and consumes ~ 6 times less.

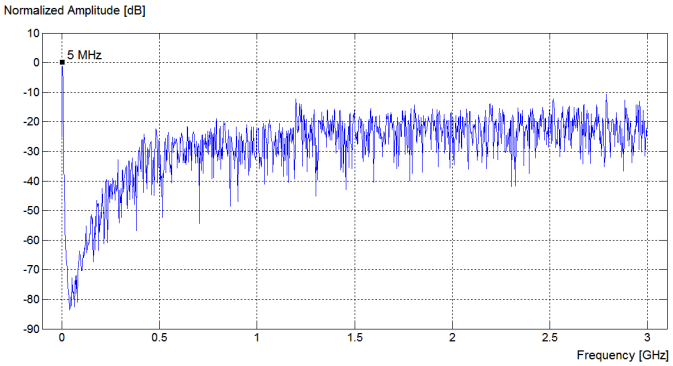

Fig. 7. Simulated output spectrum 5 channels TI DSM at 6GHz

TABLE V. SIMULATED PERFORMANCES OF TI DSM AT 4.5 GHZ

TI-channels	Supply voltage [V]	Power consumption [mW]	Total estimated Area [µm^2]
1	1.05	6.8	1 700
3	0.9	7.4	4 500
5	0.85	6.1	6 400
10	0.8	9.6	12 300
15	0.8	18.3	17 600

V. CONCLUSION

This paper presents an extended study of a delta-sigma modulator with time-interleaving that can be used as a part of a digital transmitter chain for high speed communications systems. The modulator is easily configurable in order to target large bandwidth signals up to 160 MHz, whereas the architecture choice, CIFB, is shown to be the best candidate for high frequency operation.

Furthermore, time-interleaving is proven to be effective when increasing the number of channels in order to reach higher sampling frequencies up to 6 GHz, which is 1.5 times higher than in the case of the non-TI modulator.

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