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Razvan-Cristian Marin, Antoine Frappé, Andreas Kaiser. Digital complex delta-sigma modulators with highly configurable notches for multi-standard coexistence in wireless transmitters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65 (1), pp.343-352. 10.1109/TCSI.2017.2711035. hal-02314482

HAL Id: hal-02314482 https://hal.univ-lille.fr/hal-02314482v1

Submitted on 20 Oct 2019

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Digital Complex Delta-Sigma Modulators with Highly Configurable Notches for Multi-Standard Coexistence in Wireless Transmitters

Răzvan-Cristian Marin, Student Member, IEEE, Antoine Frappé, Member, IEEE, and Andreas Kaiser, Senior Member, IEEE

Abstract—This paper presents a Complex Delta-Sigma Modulator (CDSM) designed for the integration in a digital transmitter chain targeting multi-standard coexistence with nearby receivers. The use of a Delta-Sigma Modulator (DSM) has the advantage of increased performances in terms of signal-tonoise-ratio (SNR) in the band of interest. However, the resulting out-of-band noise becomes an issue for multi-standard coexistence, thus increasing the complexity of the succeeding filtering stage. These constraints could be relaxed in the DSM stage, by placing a complex zero near the frequency band, where a low noise level is needed. This is achieved by cross-coupling the In-phase (I) and Quadrature (Q) channels, thus obtaining a CDSM. A review of known design methods for CDSM revealed limitations regarding the poles/zeros optimization, and the configurability of the complex zeros placement. The proposed architecture introduces two additional cross-couplings from the I and Q quantizers' outputs in order to decorrelate the zeros placement and the poles optimization problem. Hence, the improved CDSM can be implemented using existing optimization tools, which reduces considerably the number of iterations and the computational effort. In addition, the resulting modulator can target different coexistence scenarios without the need of redesign, unlike other known methods. Simulation results show a noise level reduction of approximately 20-30 dB near specific frequency bands by the proposed CDSM scheme with respect to standard DSM. Finally, we show an efficient fine/coarse configurability mechanism, which is obtained when introducing additional delays in the cross-coupling paths.

Index Terms—Delta Sigma Modulator (DSM), Complex Delta Sigma Modulator (CDSM), finite impulse response (FIR), multi-standard coexistence, digital transmitter;

I. INTRODUCTION

RECENT progress in advanced CMOS integrated digital transmitter (TX) architectures [1] [2] has been focusing on reducing the power consumption and circuit area to follow the trend of increased data rates and signal bandwidths (BW) in communication standards, e.g. IEEE 802.11 standard.

Furthermore, it is shown in [3] [4] that low-complexity

digital signal processing based on Delta-Sigma Modulators (DSM) can enable the use of highly-efficient power amplifier stages in a digital transmitter. Moreover, techniques such as time-interleaving (TI) [5] and multi-channel look-ahead [6] can be employed in order to overcome DSM integration challenges and increase the maximum operating frequency. As a result, it is shown in [6] that an FPGA implementation of a TI DSM-based all-digital transmitter can reach a maximum effective sampling frequency of 28 GHz and meet the transmit mask of IEEE 802.11a WLAN standard in the 5.2 GHz band.

However, there are still two important issues to be handled in digital transmitters, namely the image replicas and the outof-band noise. First of all, image replicas can be seen very close to the signal when the sampling frequency (f_s) is not high enough. For instance, in [1], for a signal bandwidth of 154 MHz, image replicas will be very close, at ±300MHz from the center frequency (f_c).

Secondly, the out-of-band noise floor injected into a nearby receiver (RX) within another band can affect the coexistence of multiple radios on the same chip.

A. Out-of-band noise vs. multi-standard coexistence

The most stringent noise specifications are found for the GPS band around 1575 MHz, due to the low typical power level of the GPS signal (\sim -125 dBm). This issue has been highlighted in [2], where a noise floor of -130 dBm/Hz is measured in the GPS band when transmitting an 802.11g 54 Mbps signal on Channel 1 with a power of 16.35 dBm. In addition, the same noise requirements apply to the GLONASS band around 1602 MHz (27 MHz away from GPS). Hence, the study of standard coexistence with GPS can be further extended to GLONASS.

In order to target advanced communication standards, [7] presents the design of a single-bit Delta-Sigma Modulator as part of a digital transmitter, focusing on time-interleaving to enable high-speed applications (up to 6 GS/s sample rate) and large signal bandwidths (up to 160 MHz).

A simple analysis regarding the two issues described before, shows that the performance of this DSM architecture is not affected by image replicas, thanks to the high sampling

Manuscript sent 08/02/2017.

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This work was supported in part by the Nano 2017 program in the frame of the ST-IEMN common lab, by STMicroelectronics, the Nord-Pas-de-Calais Region and the Research Council of the Catholic University of Lille.

frequency. It is though affected by the out-of-band quantization noise, since the main function of the DSM is to reduce the inband noise (increase SNR) by pushing it out-of-band. Hence, the amount of out-of-band quantization noise will determine the complexity of the succeeding filtering stage needed to meet stringent coexistence specifications with nearby receivers, in particular GPS/GLONASS.

One solution for the reduction of the out-of-band noise is to introduce analog filtering, which generally requires highquality passive components in order to target one specific communication standard. For example, a 6 pole LC bandpass filter [8] with the center frequency $f_c = 2.4$ GHz and a bandwidth BW = 300 MHz can achieve an attenuation of around 40 dB around the GPS band.

However, for 1-bit high-speed DSMs, a FIR-DAC based mixed-signal stage, such as the one presented in [9], offers a good alternative to analog filters. Nevertheless, the designed filter requires a large number of signal taps, resulting in area and power consumption penalty due to the implementation of coefficient cells and control logic.

In this case, the digital filtering constraints could be further relaxed in the DSM stage, by placing complex zeros near the frequency bands, where low noise levels are needed, depending on the targeted application. Still, this assumes complex nonconjugated zeros which lead to an asymmetric noise transfer function (NTF).

B. Known implementation methods of asymmetric NTF

In order to obtain an asymmetric NTF, the In-phase (I) and Quadrature (Q) channels can be cross-coupled, resulting in a Complex Delta-Sigma Modulator (CDSM) as shown in [10], where a 5th order modulator is used to match both UMTS and DCS 1800 standards out-of-band spurious emissions.

The approach in [10] combines both linear algebra and control engineering theories in order to optimize the zeros and poles placement using the state matrix, whereas the modulator is assumed to be stable if i) all the zeros are placed on the unit circle (modulus equal 1) using additional integrator feedback coefficients, and ii) all the poles are inside the unit circle and equispaced on a smaller circle centered on $z_0 = 1$ and of constant radius $r_c < 1$.

Furthermore, [11] introduces an effective design tool used to synthesize the NTF for single-path and quadrature Delta-Sigma Modulators. For a quadrature configuration, the parameters considered for the optimization are the following: the order of the NTF, the oversampling ratio (OSR), the center frequency, the rms (root mean square) in-band noise gain, the rms imageband noise gain, and the number of image-band zeros. Thus, the design methodology is simplified by obtaining an optimum and stable architecture through an iterative process based on the requirements of the quadrature DSM. A detailed description of this tool and the associated functions can be found in [12].

However, both these methods introduce limitations regarding the design of CDSM. First of all, the approach in [10] is based on large computational effort in the optimization of poles and zeros, which makes it more difficult to apply to other communication scenarios. For example, for the 5th order CDSM, the characteristic polynomial has 18 different coefficients to be set, so that the five roots (poles) can meet the poles optimization relations.

Secondly, the method in [11] cannot be used to set zeros based on noise level requirements, because the zeros placement is limited to the image-band only, which is symmetric to the transmit band with respect to f_c .

In addition, complex transfer functions have been studied also for Sigma-Delta Modulator (SDM)-based ADCs which can be used in the intermediate frequency (IF) stage of a receiver (RX). Reference [13] presents a 2nd order single-bit Complex SDM (CSDM) ADC to be used in a very low IF RX path in GSM/ GPRS/ EDGE phone applications for improved noise shaping (complex NTF), whereas only one integrator stage is complex. The coefficients of the architecture were obtained with a DSM specific design tool, because the custom complex zero is placed extremely close to the signal band (z = -0.02j), and has very little impact on the poles position.

Moreover, in [14] the SDM design concentrates on complex signal transfer functions (STF) with good stop-band attenuation, in order to reduce the image-band noise aliasing into the signal band. The algorithm is iterative and application-dependent, assuming the initial loss-pole (transmission zeros) placement derived in [15] and a minimum NTF magnitude at $\omega = \pi / OSR$.

Finally, [16] aims to reduce coefficients mismatch between the I and Q paths in a multi-bit CSDM. The method consists in adding feedback paths from the inputs and outputs of the CSDM to all the integrators inputs, which allows coefficients mismatch compensation (in digital domain) based on a matrix representation of mismatched complex operations.

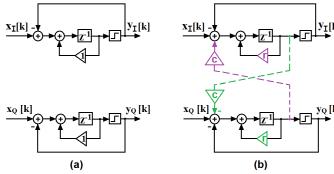
The present paper details the simplification of the design method for digital CDSM architectures, using additional crosscouplings in order to cancel the complex coefficients in the characteristic polynomial. This allows the decorrelation of the poles optimization and the zeros placement, thus eliminating the aforementioned limitations, concerning the position of the zero, the high computational effort and the lack of configurability. The modified architecture can be obtained using automatic tools with flexible custom zeros placement, for optimized out-of-band noise performances.

Section II presents the model of a 1st order CDSM, as well as the proposed modified 1st order architecture which is extended to a general approach for the design of higher order CDSM in Section III. Next, Section IV shows the flexibility of the CDSM scheme as part of a digital transmitter for multi-standard coexistence. Finally, Section V demonstrates a fine/coarse control mechanism with reduced overhead, thanks to additional delays introduced in the cross-coupling paths.

II. COMPLEX DELTA SIGMA MODULATOR MODEL

A. General architecture of 1st order CDSM

A 1st order Complex Delta-Sigma Modulator is generally obtained from two standard 1st order DSMs in quadrature, by cross-coupling the I and Q paths in order to implement an asymmetric noise transfer function (Fig. 1).





In order to ease the DSM analysis, the quantizer is often linearized by using an input-independent additive white noise model, with the quantization error sequence e[k] [17]. Performing a z-domain analysis on the linear model, we obtain $Y_I(z) + jY_Q(z) = STF(z) \cdot (X_I(z) + jX_Q(z)) + NTF(z) \cdot (E_I(z) + jE_Q(z))$ (1)

where the STF and the NTF of the standard DSM are

$$STF_{D1}(z) = \frac{1}{z} \tag{2}$$

$$NTF_{DI}(z) = \frac{z-1}{z} \tag{3}$$

and the STF and the NTF of the CDSM are

$$STF_{CD1}(z) = \frac{1}{z + (1 - r + jc)}$$
 (4)

$$NTF_{CDI}(z) = \frac{z - (r - jc)}{z + (1 - r + jc)}$$
(5)

Here, $X_l(z)$, $Y_l(z)$, $E_l(z)$ and $X_Q(z)$, $Y_Q(z)$, $E_Q(z)$ are the z-transforms of the input, output and quantization error for the I and Q paths, respectively.

The input signal is filtered by the signal transfer functions $(STF_{D1}$ for DSM and STF_{CD1} for CDSM), whereas the quantization error is shaped by the noise transfer functions $(NTF_{D1}$ for DSM and NTF_{CD1} for CDSM), in order to push the quantization noise outside the signal band. Furthermore, the NTF in (5) allows the placement of a complex zero, $z = r - jc \neq 0$, thus creating an asymmetric noise shaping based on the outof-band noise requirements. The needed complex zero can be obtained by simply replacing the coefficients r and c from (5) with the values corresponding to the targeted normalized frequency (f_n) , which can be obtained using the relationship between the z-transform and the Fourier transform in (6).

$$z = r - jc = Ae^{j2\pi f_n} \tag{6}$$

where A is the modulus of the complex number z.

Analyzing the NTF in (5), we notice a close link between the numerator and the denominator, namely the placement of a custom complex zero ($c \neq 0$) results in a characteristic polynomial with complex coefficients.

This is particularly problematic in the case of higher-order CDSM (for example 5th order in [10]), where the resulting transfer function with complex coefficients cannot be treated with design software, such as the Control System Designer toolbox in MATLAB.

Finally, this leads to two possible directions: we can either study the implementation of improved algorithms similar to [10], or propose a solution which can reduce the poles optimization to a known problem, thus allowing the use of existing design tools.

The second option, which will be further studied in this paper, suggests the decorrelation between the numerator and the denominator, by cancelling the r and c coefficients in the denominator.

B. Proposed 1st order CDSM

In order to simplify the design of CDSM, we propose to reduce the characteristic polynomial to the known case of a 1st order DSM (Fig. 1a) without affecting the placement of the custom complex zero. We can indeed introduce additional feedback paths from the quantizers' outputs to the inputs of the complex modulator. In particular, the direct feedback coefficient is modified from "1" to $a_x = r$ and a cross-coupling path with the coefficient $c_x = c$ is introduced in the modified CDSM architecture (Fig. 2).

Hence, we can obtain the STF and NTF of the proposed 1^{st} order CDSM

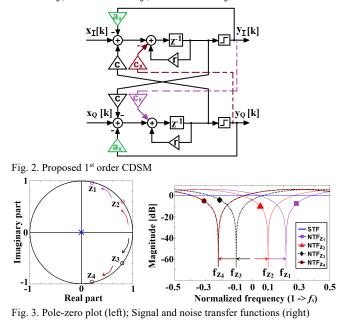
$$STF_{p1}(z) = \frac{1}{z + (a_x - jc_x - r + jc)} = \frac{1}{z}$$
(7)

$$NTF_{p1}(z) = \frac{z - (r - jc)}{z + (a_x - jc_x - r + jc)} = \frac{z - (r - jc)}{z}$$
(8)

when setting $a_x = r$ and $c_x = c$.

Therefore, using this CDSM scheme, the denominator from (7-8) is reduced to a simple delay z^{-1} (independent of *r* and *c*, no complex coefficients), whereas the numerator in (8) remains identical to (5) and enables the placement of the custom complex zero according to (6).

Thanks to the decorrelation between the zeros placement and the characteristic polynomial, the proposed architecture has the advantage of increased configurability in targeting multiple communication scenarios. This is demonstrated in Fig. 3, where the STF, NTF and the associated pole-zero plots are shown for four different custom zeros, namely $z_1 = 0.25+0.97j$, $z_2 = 0.75+0.66j$, $z_3 = 0.75-0.66j$, $z_4 = 0.25-0.97j$.



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First of all, we notice that the STF is the same for all the cases, as indicated in (7). Secondly, the sign of the imaginary part determines the position of the custom zero, namely if Im(z) > 0, then the normalized frequency is $f_z > 0$. Finally, the normalized frequency can be obtained using (6), for example in the case of $z_1 = 0.25+0.97j$, $f_{z1} \approx 0.21$.

In conclusion, this feature becomes very useful in the design of higher-order CDSM, because it allows configurable zeros placement while using existing DSM specific tools (NTF with real coefficients) for the poles optimization, which reduces considerably the number of design iterations and the computational effort.

III. HIGHER ORDER CDSM

The proposed 1st order CDSM scheme can be extended to higher order architectures in order to provide a general approach for the design of CDSMs. Thus, an n^{th} order CDSM can be built starting from (n-k) real DSM stages, followed by kcomplex DSM stages, whereas k represents the number of custom complex non-conjugated zeros that need to be added based on the targeted coexistence scenario.

This way, we can combine the advantages of both architectures, namely the increased SNR design margin thanks to the number of real stages (n-k), and the custom complex zeros placement using complex stages, respectively.

In conclusion, we can identify two CDSM cases, namely higher order CDSM with one custom complex zero, and with multiple custom complex non-conjugated zeros, respectively.

A. CDSM with one custom complex zero

Let us consider n = 4 and k = 1, namely three real stages in a Cascade-of-integrators feedback form (CIFB [11]), followed by the proposed complex integrator stage (Fig. 4).

In this case, the output in z-domain is the same as in (1), and the corresponding STF and NTF are given in (9) and (10)

$$STF_{p4}(z) = \frac{1}{den_4(z)} \tag{9}$$

$$NTF_{p4}(z) = \frac{(z-1) \cdot ((z-1)^2 + g_1) \cdot (z - (r - jc))}{den_4(z)}$$
(10)

$$den_4(z) = (z - r + a_x) \cdot (z - 1) \cdot ((z - 1)^2 + g_1) + a_3 \cdot (z - 1)^2 + a_2 \cdot (z - 1) + a_1$$
(11)

Consequently, the characteristic polynomial $den_4(z)$ presents only real coefficients when $c = c_x$, whereas the influence of r can be cancelled by the a_x coefficient.

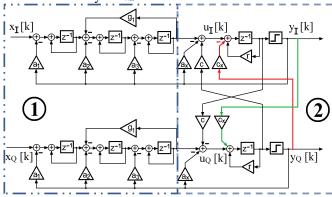


Fig. 4. 4^{th} order CDSM: three real integrators (1); proposed complex stage (2)

Thus, the decorrelation between the zeros placement and the characteristic polynomial allows the implementation of the architecture based on the coefficient set $\{a_1, a_2, a_3, a_x, g_l\}$, resulting in a design which can be reduced to a known case of standard 4th order DSM (Fig. 5), as it can be seen from the STF and NTF

$$STF_{D4}(z) = \frac{1}{den_{D4}(z)} \tag{12}$$

$$NTF_{D4}(z) = \frac{(z-1) \cdot ((z-1)^2 + g_1) \cdot (z-I)}{den_{D4}(z)}$$
(13)

$$den_{D4}(z) = (z - I + a_4) \cdot (z - 1) \cdot ((z - 1)^2 + g_1) + a_3 \cdot (z - 1)^2 + a_3 \cdot (z - 1) + a_1$$
(14)

The differences between the transfer functions of the two architectures (highlighted in Eq. (10-11) and (13-14)) show the transition from a DSM to a CDSM by moving a zero from DC (z = 1) to a custom position (z = r - jc), without affecting the optimization of the poles, i.e. the denominators of the STF and NTF are equivalent for $a_x = a_4 + r - 1$.

Hence, the proposed CDSM can be designed using existing optimization tools specific to DSM (obtain the coefficient set $\{a_1, a_2, a_3, a_x, g_1\}$), and can target different coexistence scenarios without the need of redesign, as in the case of [10] [11]. Furthermore, the multi-standard coexistence depends now on only two coefficients, *r* and *c*, making it easier to provide a configurable solution.

This design simplification is demonstrated through simulation in MATLAB of a practical example and will be described next. First of all, using the Schreier Toolbox in MATLAB, we can obtain the coefficients of a 4th order DSM, with an oversampling ratio OSR = 100 (for high-speed applications) and a peak gain of the NTF equal to 1.6. The resulting values are $[a_1, a_2, a_3, a_4, g_1] = (0.01, 0.1, 0.41, 0.93,$ 0.002), and were used to obtain the associated noise transfer function (Fig. 6), where we can observe two zeros at DC and two complex conjugated zeros at the edges of the signal band.

Secondly, as it was mentioned before, the same set of coefficients obtained for the DSM can be used in the design of CDSM with configurable custom zeros placement. In order to verify this feature, let us consider two different frequency bands, $f_{0.05} = -0.05$ (close to the signal band) and $f_{0.15} = -0.15$ (out-of-band). Using (6) we can obtain the corresponding complex numbers $z_{0.05} = 0.95 - 0.31j$, and $z_{0.15} = 0.59 - 0.81j$.

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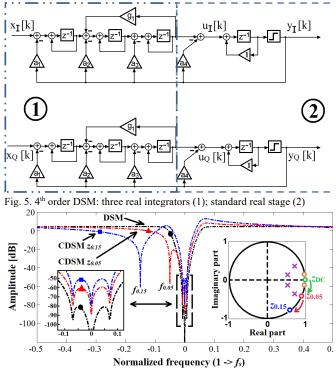


Fig. 6. 4th order DSM and CDSMs: NTFs, pole-zero plot, signal band (zoom)

These values are further introduced in Eq. (10-11) in order to obtain the NTFs shown in Fig. 6, whereas $a_{x,0.05} = 0.93 + 0.95 - 1 = 0.88$, and $a_{x,0.15} = 0.52$.

Hence, we notice that one of the zeros previously at DC is moving its position on the unit circle, depending on the values of r and c, without changing the position of the poles in all three cases (pole-zero plot in Fig. 6).

When compared to the 4th order DSM, the out-of-band noise integrated in the targeted frequency bands ($f_{0.05}$ and $f_{0.15}$) is considerably reduced in the CDSM case. However, the complex zeros placement will cause a noise redistribution leading to a degradation of SNR which becomes larger with the distance between the position of the zeros and f_c .

This effect (highlighted in Fig. 6) is specific to CDSM architectures in general, and implies a design trade-off between a reduced noise level in a specific frequency band, and overall SNR performances. This type of situation is encountered in stringent multi-standard coexistence scenarios, e.g. in a mobile application an 802.11 transmitter working in the 2.4 GHz band coexisting with a GPS receiver working in the 1.6 GHz band on the same chipset. Hence, it is important to define the SNR requirements at the beginning of the design phase and choose

the appropriate modulator's order, oversampling ratio or outof-band NTF gain, to provide adequate design margin and account for the SNR loss due to the complex zeros placement.

As can be seen, the proposed method can be applied independently of a particular value of the OSR, though reducing the OSR will inherently degrade the final SNR.

B. CDSM with multiple complex non-conjugated zeros

The implementation of a NTF with multiple complex nonconjugated zeros can be useful in applications, such as the ones presented in [10], which target the matching of the UMTS and DCS 1800 standards out-of-band spurious emissions using a 5th order CDSM with two complex integrator stages and optimized poles.

This architecture can also be implemented using the proposed 1st order CDSM scheme for n = 5, and k = 2, resulting in three real integrators followed by two complex stages (Fig. 7). Furthermore, we note that both additional cross-couplings are introduced from the I and Q quantizers' outputs, which ensures the cancellation of the complex coefficients of the characteristic polynomial without affecting the position of the custom zeros.

Next, we write the STF and the NTF

$$STF_{p5}(z) = \frac{1}{den_5(z)} \tag{15}$$

$$NTF_{p5}(z) = \frac{(z-1) \cdot ((z-1)^2 + g_1) \cdot (z - (r_1 - jc_1)) \cdot (z - (r_2 - jc_2))}{den_5(z)}$$
(16)

$$den_{5}(z) = \left[\left(z - r_{2} + a_{y} \right) \cdot \left(z - r_{I} \right) + c_{1}^{2} + a_{x} \right] \cdot \left(z - 1 \right) \cdot \left((z - 1)^{2} + g_{1} \right) + a_{3} \cdot (z - 1)^{2} + a_{2} \cdot (z - 1) + a_{1}$$
(17)

A complete decorrelation between zeros placement and poles optimization is achieved when

$$\begin{cases} c_x = c_1 \cdot (2 - a_5 - 2 \cdot r_1) \\ c_y = c_1 + c_2 \end{cases}$$
(18)

$$\begin{cases} a_x = (a_5 + r_1 - 1) \cdot (r_1 - 1) + a_4 - c_1^2 \\ a_y = a_5 + r_1 + r_2 - 2 \end{cases}$$
(19)

where a_4 and a_5 are the coefficients of the two last stages of a 5th order DSM.

Again, using the Schreier Toolbox in MATLAB we can obtain the coefficient set $\{a_1, a_2, a_3, a_4, a_5, g_1\}$ for a 5th order DSM, with an oversampling ratio OSR = 100 and a peak gain of the NTF equal to 1.6, namely $[a_1, a_2, a_3, a_4, a_5, g_1] = (0.0015, 0.018, 0.113, 0.4215, 0.93, 0.01).$

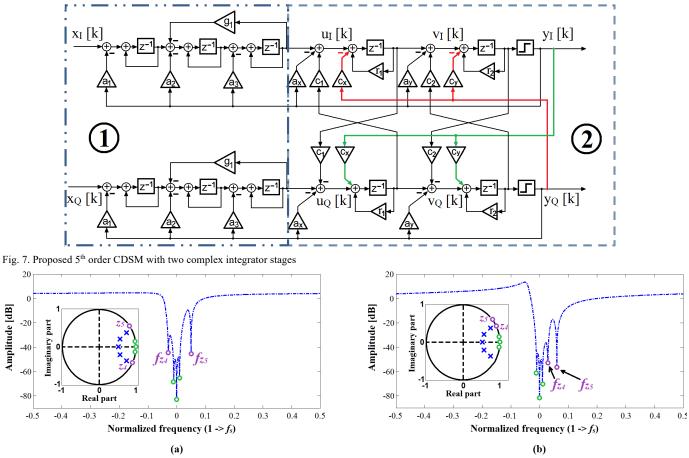


Fig. 8. NTF and pole-zero plot of proposed 5th order CDSM: a) UMTS case; b) DCS 1800 case

In order to compare the design methodology and architecture with [10], we will illustrate the functionality of the proposed higher order CDSM scheme with multiple custom complex zeros (5th order), considering the same application, i.e. UMTS and DCS 1800 standard coexistence.

In [10], for the UMTS case, the two complex non-conjugated zeros are placed in the DCS 1800 TX band at f_c -0.03, and in the UMTS RX band at f_c + 0.05, whereas for the DCS 1800 case, the first zero is placed in the DCS RX band at f_c + 0.03, and the second in the UMTS RX band at f_c + 0.06, respectively. Furthermore, in both cases there are three zeros (one real and two complex-conjugated) which are placed in the signal band, at the center frequency (f_c) and at $f_c \pm 0.01$.

By applying (6), we can obtain the complex numbers corresponding to these frequencies, namely in the UMTS case $[z_1, z_2, z_3, z_4, z_5]_{\text{UMTS}} = (1, 1+0.063j, 1-0.063j, 0.98-0.18j, 0.95+0.31j)$, and in the DCS 1800 case $[z_1, z_2, z_3, z_4, z_5]_{\text{DCS}} = (1, 1+0.063j, 1-0.063j, 0.98+0.18j, 0.93+0.37j)$. The complex non-conjugated zero pairs are $[r, c]_{\text{UMTS1}} = (0.98, 0.18), [r, c]_{\text{UMTS2}} = (0.95, -0.31), [r, c]_{\text{DCS1}} = (0.98, -0.18), [r, c]_{\text{DCS2}} = (0.93, -0.37)$. Based on these values we can obtain the NTF and the pole-zero plots for the UMTS and DCS cases (Fig. 8), which are very similar with the results presented in [10].

We remark that the design of the proposed scheme is considerably easier to perform compared to [10], while needing only the coefficient set of a DSM (obtained automatically using existing tools), and the custom zeros placement (obtained from the specifications of the out-of-band spurious emissions).

C. General CDSM design method

It was previously shown how an n^{th} order CDSM can be built out of (n-k) real stages followed by k complex stages, where $k \ge 1$. The design of the proposed CDSM can be generally reduced to the following steps (Fig. 9): i) define the SNR requirements for the desired signal bandwidths and determine the number of real stages (n-k), ii) identify the frequency bands with stringent noise requirements to obtain the number of complex stages (k)and the position of the custom complex non-conjugated zeros ([r, c] coefficient pairs), and iii) obtain the initial values of coefficients for an n^{th} order DSM with existing design tools. A simple simulation can then be performed on the chosen CDSM to verify that the SNR requirements are met.

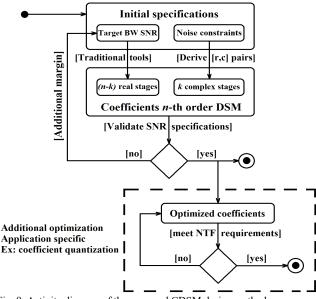


Fig. 9. Activity diagram of the proposed CDSM design method

As described previously, there is a trade-off between the inband SNR and the position of the notches relative to the center frequency. If the requirements are not fulfilled, then an additional margin is taken in the initial design phase and a new set of coefficients is generated and tested. This process requires in most application cases very few iterative steps.

Finally, we may state that the proposed method can in principle be applied to both digital (transmitter) and analog (receiver) DSM applications. Limitations remain those specific to the analog or digital domain. In the digital domain, the coefficients are subject to quantization, whereas in the analog domain the coefficients are impacted by mismatch. Mismatch between in-phase and quadrature paths can in particular be of concern in the analog implementation of complex DSMs (as shown in [16]).

IV. APPLICATION

This section details one application example in which the proposed method is used to design a 4th order CDSM as part of a highly-integrated WLAN digital transmitter chain, building upon delta-sigma modulation and efficient switching PA.

The block diagram of a DSM-based transmitter is shown in Fig. 10a, as introduced in [18]. This architecture is based on i) two single-bit DSMs working synchronously at $2*f_c$, ii) a digital to RF mixing (D-RF) stage which ideally interleaves the I and Q paths at $4*f_c$, and iii) a linear and highly efficient switching-mode power amplifier (PA). The digital implementation of the signal path up to the final PA eliminates potential I-Q mismatch and performance degradation due to this mismatch.

At the digital-to-RF mixer inputs, I and Q 1-bit samples are simultaneously available during a period $1/(2*f_c)$ as illustrated in Fig. 11a. The interleaving operation results in the sequence composed of $I(s_n)$ and $Q(s_n)$, which translates to $I(s_i)$ and $Q(s_i)$ (s_n is the sampling instant at $2*f_c$ and s_i at $4*f_c$).

However, the samples required for the RF stream RF_{out} at $4*f_c$ are I(s_i) and Q($s_i + 1$) in order to achieve a correct quadrature operation. Therefore, an interpolator stage (INT) is introduced

to derive the missing quadrature sample $Q(s_i + 1)$, which is equivalent to $Q(s_n + 1/2)$, where 1/2 represents the ratio between 2^*f_c and 4^*f_c (Fig. 11b).

A CDSM can be introduced in this architecture by crosscoupling the inner stages of quadrature DSMs (Fig. 10b), in order to place custom complex zeros and be able to target multistandard coexistence with nearby receivers.

Following the proposed CDSM design method, the first step is to define the specific SNR requirements for the targeted application, which determine the order of the CDSM. For instance, [7] describes the design of a 3rd order DSM targeting signal bandwidths from 20 MHz up to 160 MHz with an SNR larger than 67 dB.

Hence, we use three real stages followed by a complex stage to obtain a 4th order CDSM (Fig. 12) with competitive output SNR performances.

The structure is very similar to the one reported in Fig. 4, except for an additional delay of $1/(2^*f_c)$, introduced in the Q-paths from w_Q and y_Q to u_i , due to the synchronous operation of the I and Q paths of the CDSM. As explained earlier in the section, for the correct interleaving operation, the CDSM is working at half the final sampling frequency (2^*f_c) , thus producing only half the samples on each path.

Adding this delay is mandatory to process the correct I and Q samples when performing the cross-coupling of the quadrature paths.

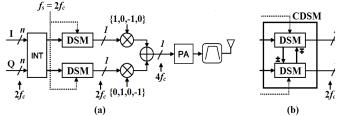


Fig. 10. Digital transmitter: (a) DSM-based [18]; (b) cross-coupled DSMs

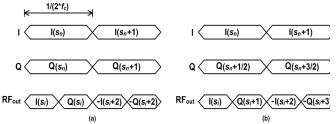


Fig. 11. D-RF stage sampling operation in [18]: (a) without INT (b) with INT

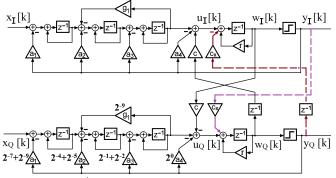


Fig. 12. Proposed 4th order CDSM as part of a digital TX chain

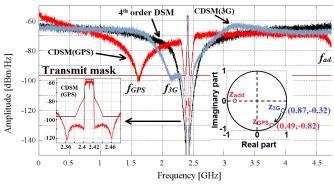


Fig. 13. Simulated output spectrum: 4th order DSM and CDSM; Complex zeros placement for 3G and GPS (zoom right)

This would not be the case if the DSM operated at 4^*f_c , yet this would imply higher power consumption and additional timing constraints as a result of the high frequency clock.

The corresponding STF and NTF of the 4th order CDSM can be expressed as follows, for $c = c_x$

$$STF(z) = \frac{1}{den(z)}$$
(20)

$$NTF(z) = \frac{(z-1) \cdot \left((z-1)^2 + g_1\right) \cdot \left(z - (r - jc \cdot z^{-0.5})\right)}{den(z)}$$
(21)

$$den(z) = a_1 + a_2 \cdot (z-1) + a_3 \cdot (z-1)^2 + (z-r+a_4) \cdot (z-1) \cdot \cdot ((z-1)^2 + g_1)$$
(22)

where a half period delay $(z^{-0.5})$ is introduced in the equation due to the additional delay elements $1/(2*f_c)$ in the Q paths, relative to the sampling period of $1/(4*f_c)$.

Consequently, using the proposed CDSM scheme, the multistandard coexistence can be made configurable and depends on only two coefficients, namely r and c, whereas the main architecture based on the coefficient set $\{a_1, a_2, a_3, a_4, g_1\}$ is the same as in the case of a real modulator. This feature is verified through simulations, for an input signal bandwidth BW = 20MHz and $f_c = 2.412$ GHz (Fig. 13). Moreover, all the coefficients are quantized to sums of powers of two in order to simplify the digital implementation.

For the same general CDSM architecture, the complex zero is placed at $f_{GPS} \approx 1.6$ GHz (close to GPS and GLONASS bands) for $[r_{GPS}, c_{GPS}] = (2^{-5}, 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4})$ in the first example, while it is placed at $f_{3G} \approx 2.17$ GHz (close to 3G communication bands) for $[r_{3G}, c_{3G}] = (2^{-1} + 2^{-2} + 2^{-4}, 2^{-2} + 2^{-4})$ in the second example, as highlighted in Fig. 13. We further observe that r has only a minor influence on the NTF. Hence, the dynamic coefficient a_x (used in Fig. 4 to compensate the real part of the complex zero in specific coexistence scenarios) can be replaced by the static coefficient a_4 of the 4th order DSM (a_4 is now used in Fig. 12 instead of a_x from Fig. 4).

When compared to the output of a 4th order DSM, the out-ofband noise integrated in the critical frequency bands (f_{GPS} and f_{3G}) is considerably reduced in the CDSM case, with ~20 dB at f_{3G} and ~30 dB at f_{GPS} . Moreover, we can notice that for the CDSM with [r_{GPS} , c_{GPS}] (CDSM(GPS) in Fig. 13) there is an additional zero at $f_{add} = 2*f_c$, which results from the second solution of the polynomial ($z - (r - jc \cdot z^{-0.5})$) in (21), namely z_{add} = -0.93 (modulus almost equal to 1). At the same time, as it was identified in a previous section, Fig. 13 reveals that the complex zeros placement leads to a relative degradation of the SNR which is proportional to the distance between the position of the zero and f_c . This degradation can be partially compensated through an adequate choice of the SNR design margin and modulator's parameters. A complementary solution may be found in [19], which proposes a 1-bit multi-step look-ahead architecture to improve the input dynamic range and SNR compared to error-feedback structures, while maintaining a low complexity overhead for real-time operation.

Furthermore, it can be seen that the bandwidth of the CDSM (zoom signal band in Fig. 13) can be configured (g_1 coefficient in Fig. 12) to address (digitally) the three non-overlapping 20 MHz WLAN channels in the 2.4 GHz band, or to increase the signal bandwidth up to 40 MHz, thus meeting the near-band transmit mask in a worst-case scenario (GPS). Finally, in order to attenuate the noise outside the CDSM bandwidth, solutions such as analog filtering, or FIR filtering [9] can be employed.

V. FINE/COARSE CONFIGURABLE CDSM

It was shown, that using the [r, c] parameters we are able to configure the complex zeros placement, whereas the frequency step (granularity) depends on the number of coefficient pairs and quantization. For example, in order to achieve configurability in the frequency domain $[f_{3G}, f_{GPS}]$ (around 600 MHz range), we need to predefine as many [r, c] coefficient pairs as possible, between $[2^{-5}, 2^{-1} + 2^{-2} + 2^{-4}]$ for r, and $[2^{-2} + 2^{-4}, 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}]$ for c, respectively.

However, this would add large constraints to a real digital implementation, due to additional paths and increased number of operations.

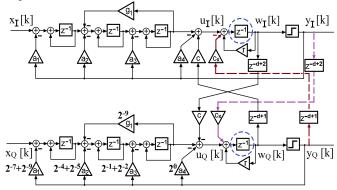


Fig. 14. CDSM with configurable delayed cross-coupling paths

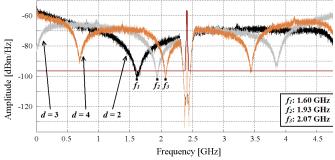


Fig. 15. Simulated output spectrum: CDSM with delayed cross-coupling paths

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In this case, the maximum operating frequency of the modulator may be reduced, thus limiting its performances (OSR, SNR, noise shaping) and application (limited f_c for the communication standard).

Consequently, we propose to minimize the number of [r, c] coefficient pairs, and combine this with a coarse tuning mechanism for band selection using additional delays in the cross-coupling paths of the CDSM (Fig. 14), similar to the principle of asymmetric embedded FIR-filtering in [20].

A. CDSM with delayed cross-coupling paths

The noise shaping of the proposed 4th order CDSM is very similar to the asymmetric unbalanced embedded-FIR filtering presented in [20], which introduces additional delays in the cross-coupled I and Q paths between the DSM and mixer stages of a digital transmitter chain similar to [18].

Furthermore, [20] employs a different number of delays in the cross-coupling paths to compensate for the INT stage, namely *d*-1 for the I (z^{-d+1}) and *d* for the Q (z^{-d}) paths ([20] uses the notation *k* instead of *d*). The main advantage of the architecture in [20] is the introduction of configurable notches at specific frequencies (based on *d*) using simple digital logic, which can relax the filtering constraints of the system.

Hence, we propose to use the same principle of delayed cross-couplings between the inner stages of the CDSM (Fig. 14), to obtain NTF notches at different frequencies.

Simulation results for an input signal bandwidth BW = 20 MHz centered at $f_c = 2.412$ GHz, $[r_{GPS}, c_{GPS}]$, and different values of d (d equal 2, 3, and 4) show that the position of the complex zero changes with d (not linear) without affecting the noise shaping around the transmit band (Fig. 15), thus providing an additional mechanism for band selection in the zeros placement.

Moreover, increasing the number of delays in the crosscoupling paths has the advantage of introducing additional notches out-of-band which relax even more the succeeding filtering stage needed to meet the overall noise requirements.

B. Fine/Coarse tuning mechanism

Let us combine the two aforementioned effects, in order to obtain a fine/coarse tuning mechanism for multi-standard coexistence, whereas the r and c coefficients are used for fine adjustment, and d is used to determine the coarse frequency band selection. In this case, using the same [r, c] coefficient pairs, we can cover several frequency domains for different values of d.

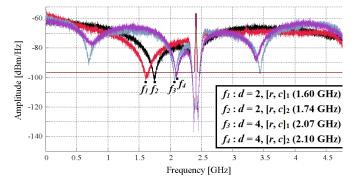


Fig. 16. Simulated output spectrum: CDSM with delayed cross-coupling paths

Let us assume N[r, c] coefficient pairs which correspond to N complex zeros which are placed in the frequency domain $[f_c - f_c/3, f_c - f_c/5]$ for d = 2. If we increase d, for example setting d = 4, we will retrieve the N complex zeros at locations which are proportional to the new frequency domain, $[f_c - f_c/7, f_c - f_c/9]$. This feature is highlighted in Fig. 16, for $d = \{2, 4\}, [r, c]_1 = (2^{-5}, 2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}), [r, c]_2 = (2^{-2} + 2^{-5}, 2^{-1} + 2^{-2} + 2^{-4})$, whereas BW = 20 MHz and $f_c = 2.412$ GHz.

Thus, the proposed fine/coarse tuning enables multi-standard coexistence in a digital CDSM-based TX chain over the frequency domain $[f_c - f_c/3, f_c]$, thanks to a reduced number of coefficient pairs combined with configurable band selection for improved performances and relaxed constraints.

In addition, this mechanism can also be applied for the symmetric frequency domain $[f_c, f_c + f_c/3]$ using only two digital inverter cells, namely for inverting the sign of the Q samples at the input of the CDSM, and again in the digital to RF mixing stage (shown in Fig. 10).

In conclusion, the complete mechanism ensures zeros placement configurability over an extended frequency domain $[f_c - f_c/3, f_c + f_c/3]$ and greatly simplifies the final architecture implementation, i.e. less coefficient pairs, digital delays for band selection and inverter cells for symmetry.

VI. CONCLUSIONS

This paper describes an improved scheme for the 1st order Complex Delta-Sigma Modulator which can be used in the design of higher order CDSMs with one or more custom complex non-conjugated zeros, using standard design and optimization tools specific to DSM.

Additional feedback paths allow the decorrelation between the placement of a complex zero and the characteristic polynomial. Hence, compared to other known methods [10] [11], the proposed CDSM can ease multi-standard coexistence using a generic well-known architecture and may achieve a noise level reduction at specific frequency bands of 20-30 dB.

Furthermore, we studied a complementary mechanism for zeros placement, by introducing additional delays in the cross-coupling paths of the CDSM block. Consequently, we obtain a fine/coarse control over the coexistence bandwidth, which simplifies the implementation, thanks to the reduced number of [r, c] coefficient pairs.

Finally, the proposed configurable CDSM presents increased flexibility and a "true" single-bit output unlike the unbalanced embedded-FIR scheme in [20], thus allowing low overhead dynamic adjustment of the complex zeros at system level to protect the relevant receive channels in the coexistence scenario.

REFERENCES

- M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, J. R. Long, "A Wideband 2x13-bit All-Digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, April 2014, pp. 732-752.
- [2] H. Wang et al., "A Highly-Efficient Multi-Band Multi-Mode All-Digital Quadrature Transmitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, May 2014, pp. 1321-1330.

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- [3] R. Hezar et. al., "A 110dB SNR and 0.5mW Current-Steering Audio DAC Implemented in 45nm CMOS," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 304-306, 2010.
- [4] R. F. Cordeiro, A. S. R. Oliveira, J. M. N. Vieira, "All-Digital Transmitter With a Mixed-Domain Combination Filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, Jan. 2016, pp. 4-8.
- [5] M. Kozak, M. Karaman, and I. Kale, "Efficient architectures for timeinterleaved oversampling delta-sigma converters," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 8, Aug. 2000, pp. 802-810.
- [6] M. Tanio, S. Hori, N. Tawa, T. Yamase, K. Kunihiro, "An FPGA-based all-digital transmitter with 28-GHz time-interleaved delta-sigma modulation," 2016 IEEE MTT-S International Microwave Symposium (IMS), pp. 1-4, May 2016.
- [7] R.-C. Marin, A. Frappé, A. Kaiser, and A. Cathelin, "Considerations for High-Speed Configurable-bandwidth Time-interleaved Digital Delta-Sigma Modulators and Synthesis in 28 nm UTBB FDSOI," in 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS), Grenoble, 2015, pp. 1-4.
- [8] Analog Devices Inc., H. Zumbahlen, "Linear Circuit Design Handbook," 1st ed., Newnes, MA 01803, USA, 2008, pp.631-633.
- [9] F. T. Gebreyohannes, A. Frappé, and A. Kaiser, "A Configurable Transmitter Architecture for IEEE 802.11ac and 802.11ad Standards," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, Jan. 2016, pp. 9-13.
- [10] C. Nsiala Nzéza, A. Flament, A. Frappé, A. Kaiser, A. Cathelin, and J. Muller, "Reconfigurable Complex Digital Delta-Sigma Modulator Synthesis for Digital Wireless Transmitters," in 4th European Conference on Circuits and Systems for Communications (ECCSC), Bucharest, July 2008, pp. 320-325.
- [11] R. Schreier. (2016, April). "Delta-Sigma Toolbox," [Online]. Available: http://www.mathworks.fr.
- [12] R. Schreier and G. C. Temes, "Understanding Delta-Sigma Data Converters," Hoboken, NJ, John Wiley& Sons, Inc., 2005.
- [13] A. Bannon, A. Dunne, D. O'Hare, M. Miller, O. Oliaei, "A 2nd Order 1bit Complex Switched Capacitor Sigma-Delta ADC with 90dB SNDR in a 180kHz Bandwidth," 13rd IEEE International Conference on Electronics Circuits and Systems (ICECS), Dec. 2006, pp. 136-139.
- [14] B. Pandita, K. W. Martin, "Designing Complex ΔΣ Modulators with Signal-Transfer Functions having Good Stop-Band Attenuation," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2007, pp. 3626-3629.
- [15] K. W. Martin, "Approximation of Complex IIR Bandpass Filters Without Arithmetic Symmetry," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 4, April 2005, pp. 794-803.
- [16] J. Marttila, M. Allen, M. Valkama, "Frequency-Agile Multiband Quadrature Sigma-Delta Modulator for Cognitive Radio: Analysis, Design and Digital Post-Processing," *IEEE J. Sel. Areas Commun.*, vol. 31, no. 11, Nov. 2013, pp. 2222-2236.
- [17] P. M. Aziz, H. V. Sorensen, and J. V. D. Spiegel, "An overview of sigmadelta converters," *IEEE Signal Processing Mag.*, Jan. 1996, pp. 61-84.
- [18] A. Frappé, A. Flament, B. Stefanelli, A. Kaiser and A. Cathelin, "An All-Digital RF Signal Generator Using High-Speed ΔΣ Modulators," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, Oct. 2009, pp. 2722-2732.
- [19] C. Basetas, T. Orfanos, P. P. Sotiriadis, "A Class of 1-Bit Multi-Step Look-Ahead Σ-Δ Modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 1, Jan. 2017, pp. 24-37.
- [20] R.-C. Marin, A. Frappé, A. Kaiser, "Delta-Sigma Based Digital Transmitters with Low-Complexity Embedded-FIR Digital to RF Mixing," 23rd IEEE International Conference on Electronics, Circuits and Systems (ICECS), Monte Carlo, Dec. 2016, pp. 237-240.



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