Digital RF transmitter architectures exploiting FIRDACs in various configurations

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Abstract

This paper discusses various ways to take advantage of semi-digital FIR filters (or FIRDACs) in highly digital RF and millimeter-wave transmitters. FIRDACs combine in a single block digital-to-analog conversion and filtering. When fed with 1-bit digital signals provided by digital delta-sigma modulators or other sources, the inherent linearity of 1 bit D-to-A converters is also preserved reducing significantly the sensitivity to component matching. Architectures using FIRDACs in base-band, IF or RF sections will be discussed, as well as opportunities for reconfiguration in highly advanced CMOS processes. Implementation examples in advanced technologies down to 28nm CMOS demonstrate the performance and scalability of these architectures.

1. Introduction

Digitizing to some extend RF transmitters has received considerable attention over le past decade. Digital processing has numerous advantages such as scalability with processes, programmability and potentially reduced circuit area compared to analog processing. It has been shown that all-digital signal generation is possible up to signal frequencies in the GHz range. Limits of the digital approach are the maximum clock rates achievable in CMOS as well as the requirements for RF digital-to-analog converters. The use of semi-digital finite impulse response filters (FIRDACs) is a way to overcome some of these limits. In particular, 1-bit implementations allow to reach high linearity while filtering significantly the out-of-band noise. In the following sections, we will review the principles of digital RF transmitters and explore different approaches for the introduction of FIRDACs in these architectures.

2. Delta-sigma modulator based digital transmitters

Delta-Sigma modulators are widely used both in AD and DA converters to quantize signals on a very low number of bits to reach high linearity and dynamic range through noise-shaping of the inherent quantization noise due to the reduction of the number of bits used for encoding the signal. The principle of a RF transmitter employing delta-sigma modulation is shown in Fig. 1.

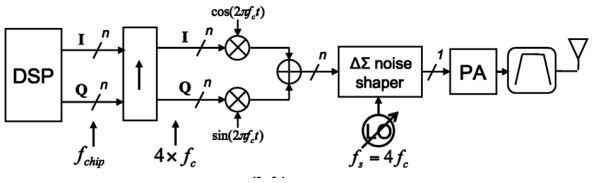

Figure 1. RF Transmitter architecture based on 1-bit bandpass Δ–Σ modulation

While band-pass delta-sigma modulators are feasible, the more common approach is to use low-pass modulators in an I-Q architecture combined with a digital mixer to reach a RF band located at ¼ of the sampling frequency [1].

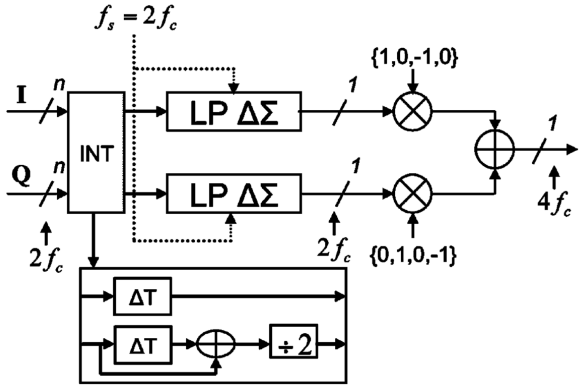

Figure 2. Optimized digital part of transmitter with 1-bit lowpass Δ–Σ modulation [1]

This approach allows to lower the sampling frequencies of the delta-sigma modulators to fs/2, and also permits time-interleaved implementations further lowering the effective sampling frequency of the digital modulators [2]. Only a small portion of the systems operates at the actual sampling frequency. The primary benefit of the architecture is an all-digital RF signal generation and perfect linearity when operated with 1 or 1.5 bit output

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signals in a differential configuration. However, the architecture suffers from large out-of-band quantization noise that requires a band-specific highly selective transmit bandpass filter. This filter is usually an external SAW or BAW filter, adding cost, complexity and lack of configurability to the system. It is therefore highly desirable to integrate these filters on chip and to achieve programmability to increase system flexibility.

3. Semi-digital FIR filters (FIRDAC)

Semi-digital FIR filters have been originally introduced in [3]. Delays of input signal are implemented in the digital domain, while multiplication with coefficients and summing are implemented in the analog domain (Fig. 3).

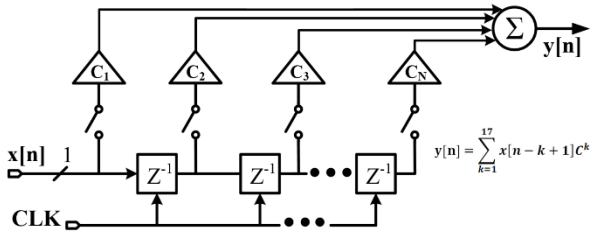

Figure 3. Principle or 1-bit FIRDAC architecture. Coefficients C1 to Cn as well as the summing operation are implemented in the analog domain.

The most common implementation uses a 1-bit input signal and switched weighted current sources to implement multiplication and current-summing in the output node (Fig. 3). The D-to-A converter is therefore embedded in the structure, and such circuits are usually referred to as FIR-DACs as they implement simultaneously filtering and DA conversion.

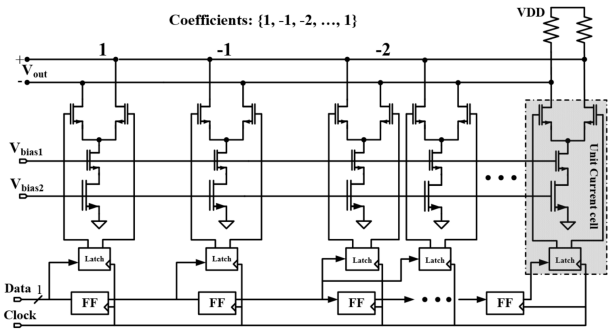

Figure 4. Typical implementation of a 1-bit current-steering FIRDAC

1-bit implementations have the advantage that matching of the individual DACs only affect the FIR transfer function without degrading linearity. Switching of current sources introduces however variable output impedance. The overall output impedance becomes therefore signal dependent and can be responsible for distortion.

An alternative to current-switching DACs are switched capacitor DACs [5]. SC-DACs provide constant output impedance as the sum of the capacitors connected to the output node remains constant, regardless of the switching state of the individual capacitors.

Finally other implementation methods have been explored at RF frequencies such as power combining with on-chip transformers [5] or transmission lines [6].

4. FIRDACs in base-band or IF band

FIRDACs can be used in the baseband or IF band for various purposes. The aim is a low power baseband or IF-band analog output signal that needs further analog processing. One example is shown in [7] for the baseband section of a WiFi transmitter suitable for 802.11ac and 802.11ad standards. Indeed, both standards aim comparable data rates, but at carrier frequencies respectively at 5Ghz and 60GHz. The 5GHz band uses a bandwidth of 160MHz with a 16 QAM OFDM modulation, while the 60GHz band uses a QPSK modulation with close to 2 GHz bandwidth available.

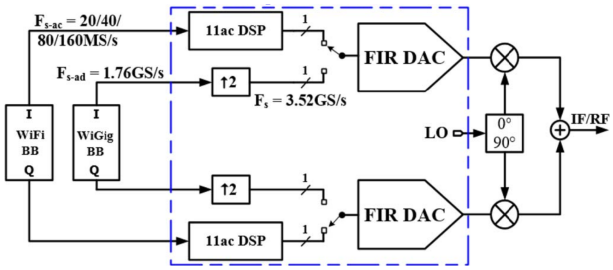

Figure 5. Dual standard 802.11ac(WiFi)/ad(WiGig) transmitter architecture based on FIRDAC

In the proposed architecture the data to be transmitted on the 802.11ac standard is encoded by a delta-sigma modulator on 1-bit stream followed by a FIRDAC eliminating the out-of-band noise in order to be transmitted on the 5GHz channel. The data to be transmitted over the 802.ad standard is simply serialized and channel filter by the FIRDAC and then transposed in two steps on the 60GHz channel. The FIRDAC sampling frequencies for both modes are identical. A re-configurable FIRDAC allows extensive hardware sharing between the two modes by simply rearranging the elementary current sources composing the FIRDAC.

While the coefficients are respectively 63 8-bit and 17 6-bit coefficients in the 2 modes, it has been shown that

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approximately 5000 unit current sources can be rearranged to implement the different transfer functions with comparable gain. The FIRDAC can also easily be adapted to support also 20MHz, 40MHz and 80MHz channels of the 802.11ac standard. The RF section remains similar to the classical Cartesian architecture, as the analog output signal is still in baseband.

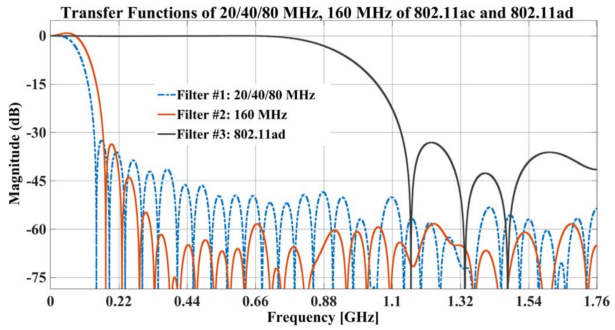

Figure 6. FIRDAC transfer functions for 802.11ac(WiFi)/ad(WiGig) modes

A variant using digital mixers prior to high-pass FIR filters can be implemented for low-bandwidth standards. The advantage is the absence of analog mixers as the analog output signal is produced at the RF frequency. As the output signal is centered at fs/4, the transmitter suffers however from significant Sinc(x) attenuation that degrades performance for the 802.11ad standard.

5. FIRDACs in the RF band

FIRDACs can also be implemented directly in the RF band. The main interest is to provide a digital architecture up to the power amplifier and reduce requirements for off-chip filtering.

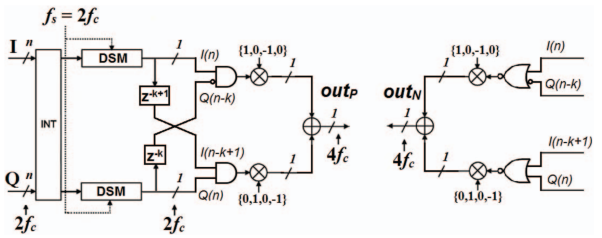

Figure 7. Digital implementation of a complex transmission zero in a 1.5-bit architecture.

In a differential version of the architecture of Fig. 2, simple programmable delays can be introduced to introduce a FIR function without any further modification of the architecture introducing a programmable transmission zero (Fig. 7 & Fig. 8).

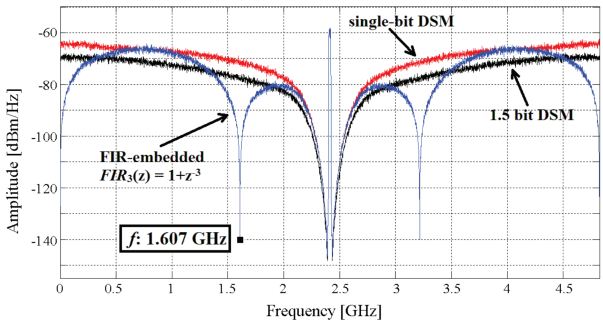

Figure 8. Principle of 1-bit Power-FIRDAC using a transmission line based power combiner.

Thanks to the complex signal representation, the additional zero can be arbitrarily placed and the transfer function does not need to be symmetric. The noise floor in the signal band is not modified as the architecture is in practice transformed from a differential 1-bit architecture to a 1.5 bit architecture. All properties of the differential 1-bit architecture are preserved. Fig. 7 compares the 1-bit, the theoretical 1.5 bit and the FIR-filtered output spectra, showing that the additional 0.5 bits are used to introduce the additional notch in the transfer function.

The FIR filtering function can also directly be merged in the power stage at the RF output. The main interest is to provide a digital architecture up to the power amplifier and to exploit power combining techniques to implement the FIR function.

[6] uses five 1-bit PDACs and a transmission-line based power combiner (Fig. 9). The output power in the signal band is constructively summed, while other frequencies are filtered out.

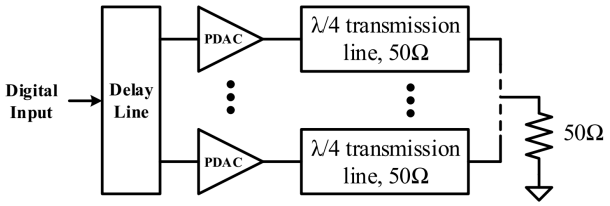

Figure 9. Principle of 1-bit Power-FIRDAC using a transmission line based power combiner.

Associated to a Δ–Σ based digital RF signal generator [1] it provides a fully digital transmitter up to the matching network. A practical implementation models the transmission lines by lumped elements that can be integrated on-chip or on-package. The output seen in Fig. 10 demonstrates the effectiveness of the quantization noise filtering by the relatively simple system architecture.

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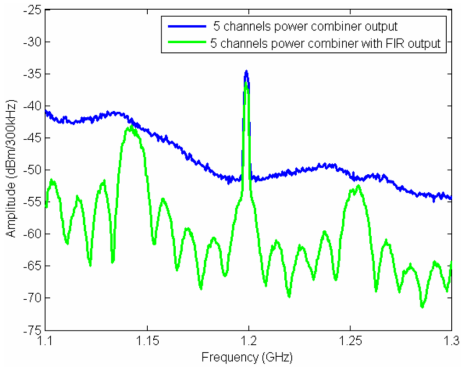

Figure 10. Output spectrum with and without enabling the FIR function. The peak output power is 18dBm

More recently, a similar architecture using transformer based power combining has been shown [5]. Four switched-capacitor based multi-bit PDACs drive a differential 2-to-1 power combiner. I&Q signal are directly summed at the DAC outputs. Introducing delays between the four signal phases implements a filtering function that reduces the noise in adjacent signal bands. The peak power reached is 30.3 dBm, while the FIR reduces the noise floor in critical bands by about 20dB. A duplexer/band filter is still necessary in this approach to meet the stringent noise requirements in the receive band.

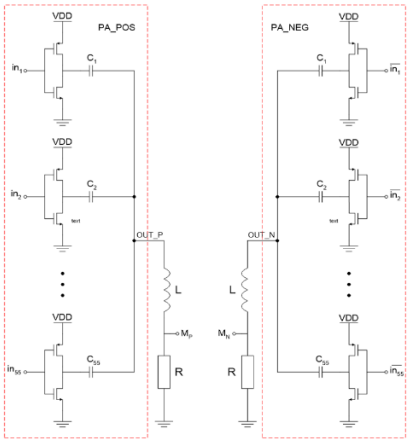

Figure 11. Principle of a differential 1-bit 55thorder FIR SC-PDAC

SC-PDACs (Fig. 11) can also be used to implement high order FIR function by driving the switches with delayed versions of the input signal and FIR coefficients implemented by the capacitor values. This will allow a fully digital implementation of the architecture of Fig. 1 up to the antenna able to address power levels on the order of 20dBm. The capacitors form a passive LC bandpass filter with the series inductance, which should help to eliminate any need of costly external passive filters.

6. Summary

This paper reviewed the use of FIRDACs in highly digital transmitter architectures. Recent advances open the road for fully digital implementation of RF transmitters in advanced nanometer CMOS technologies with a minimal number of external components

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