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Keywords

≪Gallium Nitride (GaN)≫, ≪Double pulse test≫, ≪Device characterisation≫, ≪Switching losses≫, ≪Threshold voltage shift≫

Abstract

A new method is proposed in this paper to investigate the influence of current collapse effect on the I_d-V_{ds} characteristics of GaN-HEMTs in high voltage region based on a modified H-bridge circuit. The measured I_d-V_{ds} characteristics with and without the V_{ds} bias are compared, which shows the effect of charge trapping due to the V_{ds} bias on device I_d-V_{ds} characteristics in saturation region. These data will be used for a device model including the current collapse effect in full I_d-V_{ds} region.

Introduction

Gallium Nitride High-Electron-Mobility Transistors (GaN-HEMTs) are strong candidates for high-power-density and high-efficiency power converters due to the fast switching speed and low power losses. To accurately model the switching transients of high voltage GaN-HEMTs, an appropriate drain-current versus drain-source voltage (I_d-V_{ds}) characteristics covering the entire switching trajectory is indispensable. However, the I_d-V_{ds} characteristics provided by the datasheet are only in low V_{ds} voltage region of few volts which cannot predict the high voltage switching trajectory. The reason is that most of the I_d-V_{ds} characteristics are measured by curve tracer, which is not suitable for high voltage measurement due to the equipment power limitation. Moreover, GaN transistors suffer from the current collapse effect due to the trapped electrons in device structures induced by the off-state V_{ds} bias, on-state V_{gs} bias and hot electrons, which degrades device characteristics resulting in the increased dynamic on-state resistance (R_{dson}) and the threshold voltage (V_{th}) shift [1], [2]. Many research work focused on the device dynamic R_{dson} degradation in Ohmic region, which increases device conduction losses [3–5]. But there is not much reported data for this characteristics degradation under saturation region, which though is highly relevant to the device switching waveforms and switching losses. The impact of current collapse on the device turn-on losses are reported in [6], which may be attributed to a positive V_{th} shift, but there is no quantitative study on characteristics shift. This characteristics shift will have an impact on device switching transients, which may increases switching losses, trigger sustained oscillation etc [10]. Furthermore, the main advantage of GaN-HEMTs is the high frequency application so the influence of current collapse effect on device switching transients deserve much attention. Consequently, it is necessary to have a method to construct the I_d-V_{ds} characteristics of GaN-HEMTs in high voltage region and investigate the current collapse degradation in saturation region.

This work proposes a new method to measure the I_d-V_{ds} characteristics of GaN-HEMTs in high voltage region, which is based on a modified H-bridge to control the V_{ds} initial voltage bias. The I_d-V_{ds} characteristics are extracted from the turn-on switching waveforms during the whole Miller plateau. In order to reduce the influence of circuit parasitic inductance (L_{para}) and device output capacitance (C_{oss}) on measurement results, a large turn-on gate resistance (Rg_{on}) is used to slow down the switching-on speed. The I_d-V_{ds} characteristics are compared between a fresh device, referred to as unbiased (short: ub) and a device after V_{ds} voltage bias (short: b), which are recorded respectively as I_d-V_{ds}^{ub} and I_d-V_{ds}^{b} characteristics to demonstrate the V_{ds} bias effect. The paper is constituted by following parts. At first, the proposed experimental setup to measure the high voltage I_d-V_{ds} characteristics are presented. Afterward, the influence of circuit L_{para} and device C_{oss} on measurement results as well as device self-heating are analysed. In the third section, the measured I_d-V_{ds}^{ub} and I_d-V_{ds}^{b} characteristics are compared, in which a positive shifted V_{th} and the decreased current in high-voltage saturation region are observed. The paper is concluded at last with a discussion on future work.

Experimental setup

To investigate the influence of current collapse of GaN-HEMTs on saturation region, it is essential to have an experiment that can not only measure the high voltage I_d-V_{ds} characteristics but also control the V_{ds} initial bias, which is highly related to current collapse effect aforementioned. Several research works have focused on constructing the I_d-V_{ds} characteristics of SiC MOSFETs in high voltage region based on the double-pulse test [7], [8]. In [7], the high voltage I_d-V_{ds} characteristics are constructed from measured I_d and V_{ds} points, where V_{gs} equals to the Miller plateau voltage (V_{pl}). The drawback is that only one data point can be acquired per test and each test requires different settings to obtain different V_{ds} and I_d values. More importantly, this method do not control initial V_{ds} bias of the DUT, which is not suitable for GaN-HEMTs characterization because the initial V_{ds} bias can affect device characteristics as mentioned before. In [9], a circuit to control the initial V_{ds} bias induced trapping effect of GaN-HEMTs in conventional DPT is proposed, but the impact on full I_d-V_{ds} characteristics of the device is not mentioned. Overall, two advantages of the proposed method are that the initial V_{ds} voltage bias can be controlled to avoid the V_{ds} trapping effect and less tests are required as only I_d needs to be adjusted during each test.

The experiment board consists of a main DPT board and an auxiliary board as shown in Fig. 1(a), which is proposed in [10] at first. Point A and B are not hard-connected as the conventional DPT board, which can be separated by the T_H to avoid the initial drain bias of DUT. Hence, this experiment board supports two test modes as detailed below.

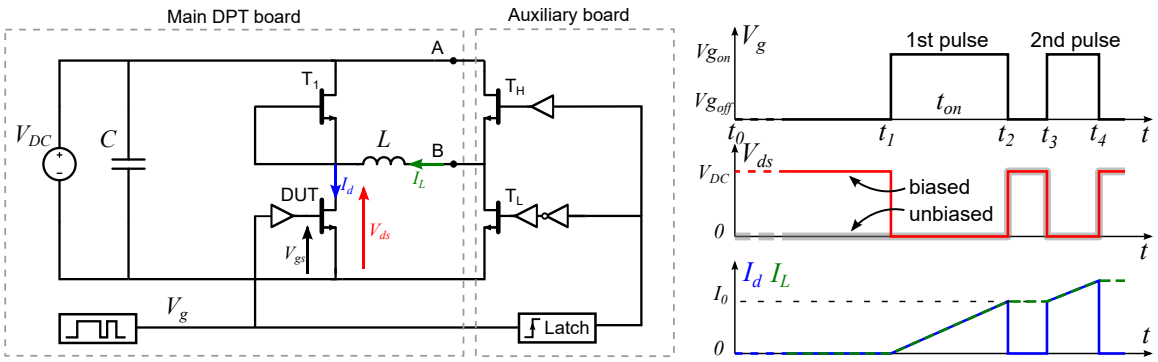
Conventional DPT mode

Under this mode points A and B in Fig. 1(a) are connected, therefore, the experiment board will work in the conventional DPT mode. The top-side device T_1 works as a freewheeling diode by shorting the gate and source terminal. The voltage drop and current flowing through the DUT are V_{ds} and I_d respectively.

The DUT is controlled by a double-pulse signal V_g as shown in Fig. 1(b). From t_0 to t_1, the DUT is in turn-off state undertaking DC source voltage, called the initial drain bias. At t_2, the inductive load is charged and I_d is the same as load current I_L, which can be calculated by equation (1):

$$I_d = I_L = V_{DC} \times \frac{t_{on}}{L} \tag{1}$$

In eq(1), L is the load inductance and t_{on} equals to t_2 - t_1. The time interval between t_2 and t_3 is short, and the load current is freewheeling through transistor T_1 during t_2 - t_3. Thus, the turn-off and turn-on switching transient of the DUT at same current and voltage can be observed at t_2 and t_3. Moreover, the commutation speed at turn-on and turn-off of the DUT can be adjusted by using different gate resistor Rg_{on} and Rg_{off}. However, the DUT under this mode undertakes V_{ds} voltage bias before the test is



(a) (b)

Fig. 1: Experimental setup. (a) Schematic of experimental setup. (b) Typical waveforms of experimental setup.

started at t_1, therefore, the obtained DUT turn-on and turn-off switching waveforms include the V_{ds} bias effect [11]. To compare with the switching waveforms without V_{ds} bias effect, an unbiased mode of the modified DPT will be introduced below.

Unbiased DPT mode

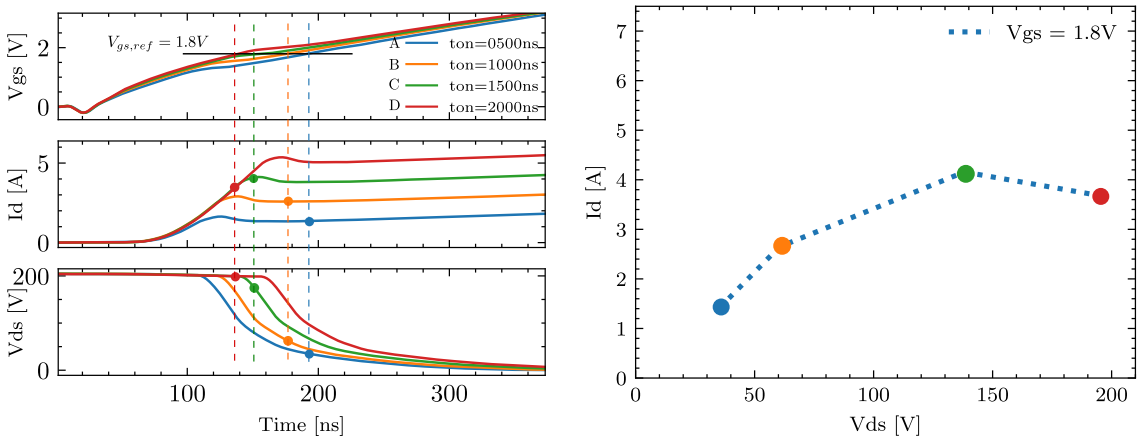
When A and B in Fig. 1(a) are separated by auxiliary board, the experiment board will work in unbiased DPT mode. The top-side device T_H in auxiliary board is synchronously controlled with DUT by V_g while the low-side device T_L is complementary to the T_H by adding a NOT gate in the driver side. Before test starting (during t_0 - t_1), DUT and T_H are in off-state and T_L is turned on, so the DUT is free of the initial drain bias since T_H blocks V_{DC} for the DUT. Afterward, during the rising edge of the first pulse at t_1, the transistors in auxiliary board are latched (T_H and T_L are in on and off state respectively) and the modified DPT board will resume to conventional DPT operation as shown in Fig. 1(b).

The proposed method to obtain high voltage I_d-V_{ds} characteristics is established on the Miller plateau of turn-on switching waveforms. To clearly show the Miller plateau and eliminate the impact of parasitic circuit elements, a large Rg_{on} = 1 kΩ is chosen to slow down the turn-on switching speed. All power transistors in the H-bridge are GaN devices (GS66502B 650 V/7.5 A). The V_{gs} of DUT are measured by a 500 MHz passive probe (N2873A) and the V_{ds} is measured by a high voltage differential probe (N2790). A current probe (N2783B) is used to measure the I_d. The DC source voltage is set at 200 V, which determines the V_{ds} range in measured I_d-V_{ds} characteristics. And I_d can be controlled by adjusting the duration of the first pulse t_{on} based on equation (1). Therefore, full current and voltage of DUT can be obtained. These setup will be implemented in both conventional DPT mode and unbiased DPT mode to get two sets of data, to investigate the influence of drain bias on device I_d-V_{ds} characteristics in saturation region.

Measurement results and error analysis

Measurement results

Turn-on switching waveforms of the DUT measured in the unbiased DPT mode are shown in Fig. 2(a), where curve A, B, C and D respectively represent different switching waveforms (V_{gs}, I_d and V_{ds}) with incremental t_{on} from 500 ns to 2000 ns. The I_d and V_{gs} keep nearly constant while V_{ds} decrease during the Miller plateau so that different I_d and V_{ds} data with the same V_{gs} can be obtained in this region. For example, when $V_{gs,ref}$ = 1.8 V, it has an intersection with curve A (t_{on} = 500 ns) and the corresponding I_d and V_{ds} point can be obtained, which is one measured point. As $V_{gs,ref}$ has other intersections with different V_{gs} from curve B, C, and D, a set of measured points can be obtained, which consists an I_d-V_{ds} curve with V_{gs} = 1.8 V as shown in Fig. 2(b). By repeating this over a range of $V_{gs,ref}$ values, the high voltage I_d-V_{ds}^{ub} characteristics with different V_{gs} can be obtained. Correspondingly, if the switching waveforms are from conventional DPT, a high voltage I_d-V_{ds}^{b} characteristics can be obtained.



(a) (b)

Fig. 2: High voltage I_d-V_{ds} measurement principle. (a) Turn-on switching waveforms for different t_{on} from 500 ns to 2000 ns. (b) I_d-V_{ds}^{ub} characteristics at V_{gs} = 1.8 V.

The I_d-V_{ds} characteristics measurement method using curve tracer is steady-state measurement, where the channel of DUT is completely formed before drain current flowing through it, which may not correspond to the real switching process of device and involves significant self-heating. While the proposed method is based on device turn-on switching transient, which follows a real dynamic V_{ds}, I_d and V_{gs} trajectory of the DUT in hard-switching, with low self-heating. However, even with slow commutations the GaN device switching transients remain sensitive to parasitic circuit elements, and the junction temperature might still noticeably increase and influence the I_d-V_{ds} data for high voltage and current values. Thus, it is necessary to discuss and quantify these impacts.

Error analysis and compensation

There are several factors (e.g., measurement noise, parasitic circuit elements, device output capacitance and junction temperature) that can affect measured results, which will be discussed in the following parts.

Measurement noise

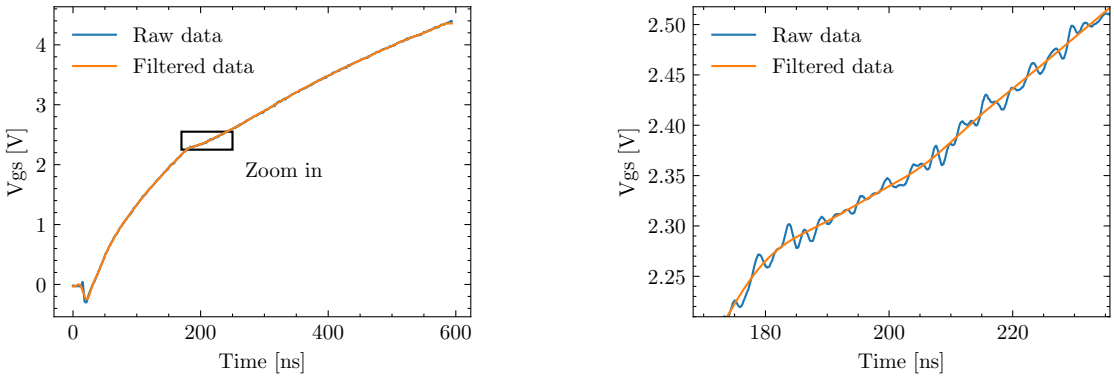
Accurate intersections of a fixed V_{gs} value and measured V_{gs} waveforms in Fig. 2(a) are significant in this method. However, measured V_{gs} waveforms are affected by measurement noise as shown in Fig. 3, which may interfere the location of intersections, leading to inaccurate V_{gs}, V_{ds} and I_d values. The noise frequency is mainly above 60 MHz according to the signal spectrum analysis. A Butterworth filter with 60 MHz cut-off frequency is used to filter the high-frequency measurement noise based on the zero-phase filtering method. The filtering result is shown in Fig. 3(b). Note that all of the measured V_{gs}, V_{ds} and I_d are filtered using this method to improve the accuracy of high voltage I_d-V_{ds} characteristics.

Influence of parasitics parameters

The I_d-V_{ds} characteristics represent the relation between the device channel current I_{ch} and the voltage drop on gate-source capacitance V_{Cgs}. However, the I_{ch} and V_{Cgs} cannot be directly measured in DPT due to the parasitic elements in device packaging as shown in Fig. 4(a). Therefore, the impact of these parasitic parameters on the difference between measured I_d, V_{gs} and device internal I_{ch}, V_{Cgs} should be discussed.

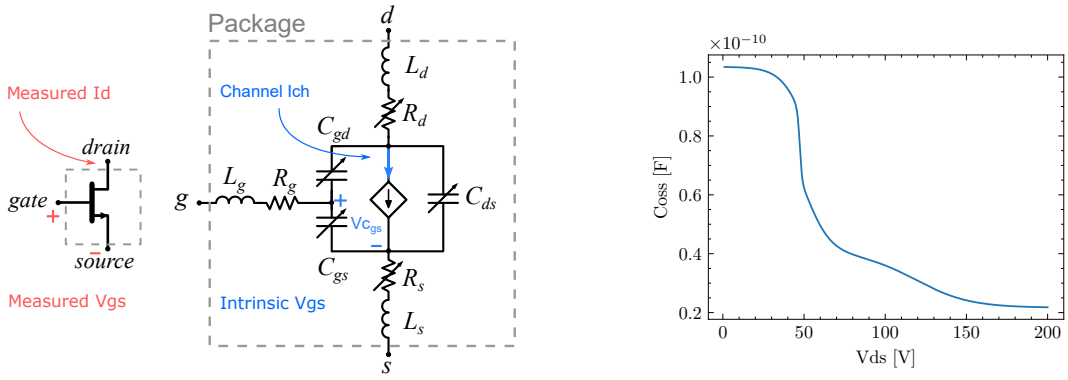
During the turn-on transient, the $C_{oss} = C_{gd} + C_{ds}$ of the DUT will discharge and the corresponding I_{Coss} current cannot be measured by current probes. Hence, the I_{Coss} should be calculated to compensate measured I_d as equation (2) shown.

$$I_{ch} = I_d + I_{Coss} = I_d + C_{oss}\frac{dV_{ds}}{dt} \tag{2}$$



(a) (b)

Fig. 3: V_{gs} waveform with and without filtering. (a) V_{gs} waveform in turning-on. (b) Zoomed-in V_{gs}.



(a) (b)

Fig. 4: Parasitic elements inside the device package. (a) Symbol and device parasitic elements of GaN-HEMTs. (b) C_{oss} - V_{ds} of GS66502B.

C_{oss} is a non-linear capacitance, which is V_{ds} voltage dependent. An accurate C_{oss} model of GS66502B is presented in [12] as shown in Fig. 4(b), which is used to calculate I_{Coss}.

As shown in Fig. 4(a), the measured V_{gs} is the potential between gate and source terminals including the voltage drop on the L_g, L_s and R_g, R_s. Moreover, the mutual inductance between power loop and gate loop M_p will also exert additional voltage drop on measured V_{gs}. These voltage drops should be compensated to get the V_{Cgs}. The impact of parasitic inductance L_g, L_s and mutual inductance M_p can be neglected because the low $\frac{dI_d}{dt}$ during Miller plateau and the value of L_g and L_s are at most several hundreds pico Henry [13]. As for the internal gate resistance R_g, the voltage drop is determined by the gate current I_g that can be calculated by equation (3).

$$I_g = \frac{V_g - V_{Miller}}{R_{gon}} \tag{3}$$

Where the output voltage of gate driver V_g is 6 V and the minimal V_{Miller} is about 1.5 V (based on measurement) and R_{gon} is 1 kΩ. So the maximum I_g is around 4.5 mA. According to the device model from manufacturer, the R_g is 225 mΩ so the voltage drop is around 1 mV, which can also be neglected. Hence, the difference between measured V_{gs} and intrinsic V_{Cgs} is the voltage drop on the R_s, which can be compensated based on equation (4).

$$V_{Cgs} = V_{gs} - (I_d + I_g)R_s \tag{4}$$

R_s is considered to be constant (14.3 mΩ) because of the extreme low temperature sensitivity (0.1 mΩ/K)

based on the result in [13]. Consequently, the error between measured I_d, V_{gs} and device internal I_{ch}, V_{Cgs} can be compensated by the above method.

The comparison of the measured I_d-V_{ds} characteristics with and without the error compensation are shown in Fig. 5. The influence of the measurement noise and parasitics parameters on the high voltage I_d-V_{ds} characteristics are obvious in high current region.

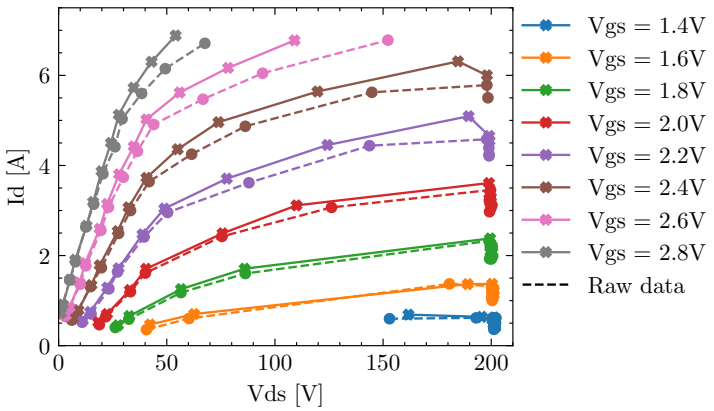


Fig. 5: I_d-V_{ds}^b characteristics with and without error compensation from conventional DPT.

Self-heating of the DUT

During the measurement, the DUT will turn on and off twice as shown in Fig. 1(b). The turn-off switching speed is fast as a small Rg_{off} is used, which will not cause much switching losses. However, a large Rg_{on} is used to slow down the turn-on speed, which may cause noticeable self-heating.

The RC thermal SPICE model of GS66502B provided by the datasheet is adopted to estimate the junction temperature T_j during the measurement, which is shown in Fig. 6. Where the R_n and C_n represent the thermal resistance and capacitance of different layers in the device package, and the R_{CA} represents the thermal resistance between case and ambient. The T_j and T_c are the junction and case temperature respectively. The ambient temperature is set to 25 °C. The T_j can be calculated when the device power losses are imported into this model as the power source.

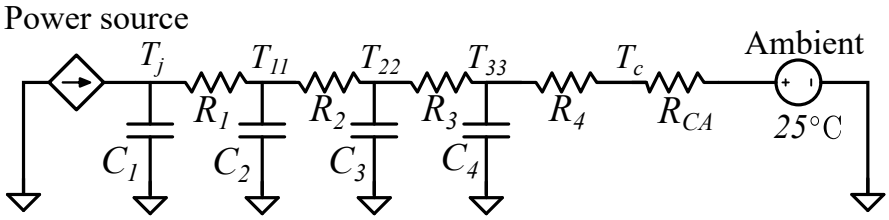
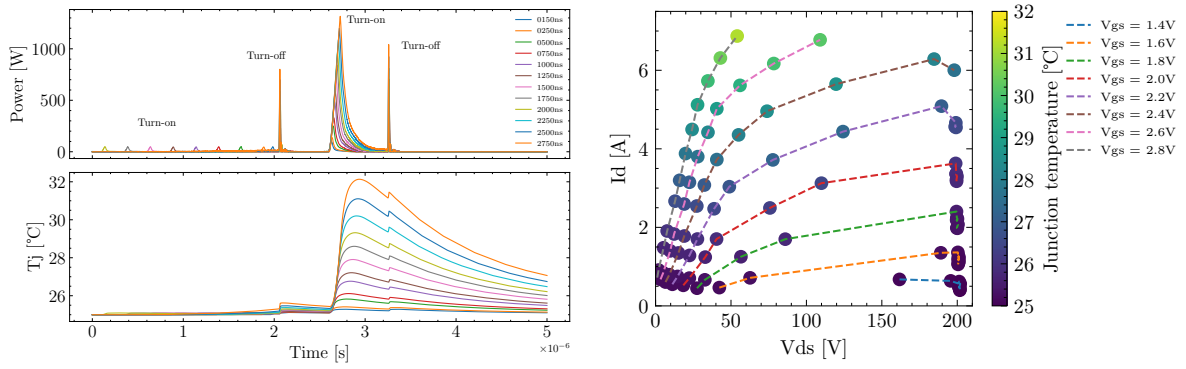


Fig. 6: RC thermal model simulation.

As shown in Fig. 7(a), only the second turn-on transient causes obvious switching losses and increased temperature. And the first turn-on loss can be neglected in both unbiased and conventional DPT mode because the first turn-on transient is zero current switching (ZCS). Hence, the increased T_j is mainly caused by the second turn-on transient, which is similar in unbiased model and conventional DPT mode. Note that the initial values of T_j at the second turn-on transient are different as a result of the heat accumulation from previous switching losses. This is due to the large thermal propagation time constant R_2C_2, which slows down the temperature propagation speed from junction to case. Anyhow, the maximum change of T_j is less than 7 °C, which validates that R_s can be considered as a constant resistance during the test.

Based on the processed V_{gs}, I_d, V_{ds} and T_j, a high voltage I_d-V_{ds}^b characteristics with temperature distribution can be obtained in Fig. 7(b), where the temperature variation is small even in high voltage region, so the measured I_d-V_{ds} characteristics can be seen as in constant temperature.

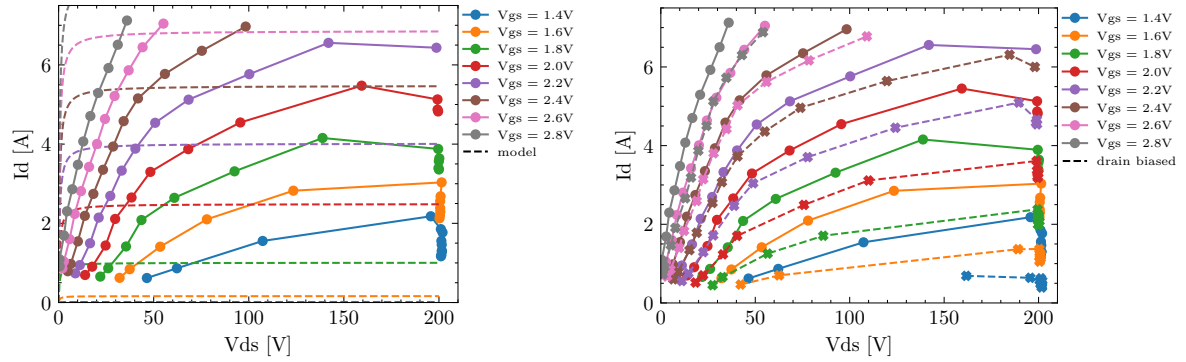


(a) (b)

Fig. 7: Junction temperature and high voltage I_d-V_{ds}^b characteristics from conventional DPT. (a) Power and T_j versus time. (b) Temperature distribution in I_d-V_{ds}^b characteristics.

Influence of drain bias on measured I_d-V_{ds} characteristics in saturation region

The high voltage I_d-V_{ds}^{ub} characteristics constructed from the unbiased DPT mode are expected closer to the original device characteristics because there is no initial V_{ds} bias. Thus, the I_d-V_{ds}^{ub} characteristics are compared to the simulation result from the manufacturer model, which are shown in Fig. 8(a). Note that the I_d-V_{ds} characteristics of the manufacturer model is the same as that in the datasheet. The measured I_d-V_{ds}^{ub} characteristics has a noticeable difference with it in the manufacturer model, which mainly represents as higher I_d in saturation region. Since the switching trajectory is mainly located on the saturation region and it is highly related to switching losses, it is reasonable to assume that in the real working condition the device switching losses are different with that predicted by simulation using the manufacturer model.

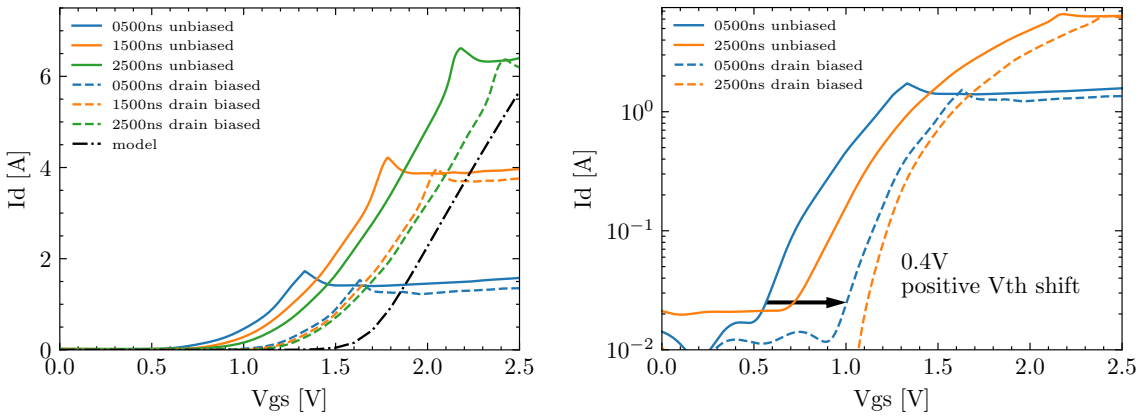


(a) (b)

Fig. 8: I_d-V_{ds} characteristics comparison. (a) Measured I_d-V_{ds}^{ub} characteristics versus manufacturer model. (b) Comparison of I_d-V_{ds}^{ub} and I_d-V_{ds}^b.

Measured I_d-V_{ds}^b and I_d-V_{ds}^{ub} characteristics are compared in Fig. 8(b). A distinct decreased current is observed in the drain biased condition, which reveals the drain bias trapping effect on saturation region. This comparison shows a clear perspective that the drain bias trapping effect can affect device switching losses by changing the device switching trajectory.

Moreover, the device transfer characteristics from different measurement modes and manufacturer model are compared in Fig. 9. As shown in Fig. 9(a), the measured transfer characteristics has an negative shift compared with the manufacturer model (when V_{ds} is 10 V). On the other hand, the drain biased transfer characteristics at $V_{ds} = 200$ V have a positive shift compared with the unbiased transfer characteristics. To quantify these shifts, the I_d is represented on the logarithmic axis as shown in Fig. 9(b). The V_{th} of device is determined when I_d is above 20 mA. A 0.4 V positive V_{th} shift is observed between the unbiased and



(a) (b)

Fig. 9: Transfer characteristics comparison when V_{ds} = 200V. (a) Measured transfer characteristics versus manufacturer model. (b) Transfer characteristics with and without drain bias in logarithm scale.

biased transfer characteristics when the first turn-on pulse time t_{on} = 500 ns. In addition, a slight positive V_{th} shifts are observed when t_{on} increases from 500 ns to 2500 ns in both biased and unbiased transfer characteristics. The positive V_{gs} bias induced trapping effects may contribute to this V_{th} shift since the t_{on} is positively correlated to the positive V_{gs} bias time during the first turn-on pulse as shown in Fig. 1(b). Additionally, the positive V_{th} shift of GaN-HEMTs under positive V_{gs} bias was reported in [14], [15].

It should be noted that the turn-on speed of the DUT is very slow for a GaN device due to the large turn-on gate resistance, hence, the overlapping of the V_{ds} and I_d waveforms is larger than that in the normal turn-on transient, which provides more opportunities for hot electrons trapping to occur in device structure. However, the hot electrons trapping and voltage biased trapping are coupled together in this measurement setup. Consequently, it is necessary to have the quantitative characterization for the hot electrons and V_{gs} bias trapping effect separately. The constructed I_d-V_{ds} characteristics and the trapping effect will be considered in device modelling in our future work.

Conclusion

This paper proposed a new method to evaluate the influence of current collapse effect on the I_d-V_{ds} characteristics of GaN-HEMTs in high voltage region. The influence of measurement noise, parasitic circuit elements and junction temperature are considered and they are extracted to obtain the I_d-V_{ds} characteristics representing the relation between channel current and gate source voltage. The I_d-V_{ds}^{b} and I_d-V_{ds}^{ub} characteristics are compared and the decreased current in high voltage region and positive V_{th} shift in transfer characteristics are observed. The future work will focus on device modelling based on the measured data, which will consider both of the voltage bias and hot electron trapping effect in the full I_d-V_{ds} range to enhance the accuracy of simulated switching waveforms of GaN-HEMTs.

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