# PWM Strategy for the Cancellation of Common-Mode Voltage Generated by Three-Phase Back-to-Back Inverters

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***Abstract*—This paper presents a PWM strategy for the cancellation of common-mode (CM) voltage generated by three-phase back-to-back two-level inverters. This method theoretically provides complete elimination of the CM voltage by synchronizing all the commutations of one converter with commutations of the other one, so that the overall resulting CM voltage does not vary. The degrees of freedom of this strategy are studied and an experimental implementation is carried out on a 15 kW motor drive prototype to validate the method effectiveness. Taking into account dead-time compensation, measurements in time and frequency domains show that the CM voltage is strongly reduced and that more than 15 dB reduction is achieved in a wide frequency range.**

***Index Terms*—Pulse width modulated inverters, Variable speed drives, Rectifiers, Electromagnetic compatibility, Electromagnetic conductive interference**

## I. Introduction

THREE-PHASE voltage-source inverters are a major source of electromagnetic interferences (EMI) due to the fast switching of their power semiconductors [1]. Especially, a common-mode (CM) voltage is generated between the input and output potentials of the converter, inducing CM currents because of parasitic capacitive coupling to the ground in power cables and electric motors in variable-speed drives (VSDs) applications [2], [3]. As a consequence, high levels of conducted perturbations are emitted toward the power grid, which exceed the limits imposed by electromagnetic compatibility (EMC) standards. As a consequence, costly and bulky EMI filters are usually necessary, at least on the grid side of VSDs [4]. Another harmful effect of CM voltage is the generation of shaft voltage across the motor bearings that may cause destructive electric discharge machining [5], [6]. In order to prevent EMI on the load side, output EMI filters may be necessary, adding to the total cost and weight of the converter.

Acting on the converter PWM strategy is an interesting solution to these issues. Indeed, with low overcost it is possible to reduce the source of perturbation by performing simultaneous commutations so that their effects on CM voltage cancel each other. Such CM-voltage-reducing PWM strategies have been proposed for three-phase matrix converters [7], [8], dual converters for open-end windings motors [9], and single two-level [3] and multilevel inverters [10]–[15], usually with drawbacks regarding the DC bus utilization or output power quality (current ripple, motor overvoltages in long cable applications) [16], [17]. Indeed, CM cancellation is performed by simultaneous switching in opposite direction of two legs, resulting in increased phase-to-phase voltage steps. In this regard, multilevel converters are interesting as they naturally improve the differential-mode voltage quality. On the other hand, little research has focused on the back-to-back voltage-source inverter topology [18]–[20], where the typical diode-bridge rectifier in VSDs is replaced with a PWM rectifier (active front-end, Fig. 1). In this case, simultaneous switching in the same direction of one inverter leg with one rectifier leg allows CM voltage cancellation of the whole association of two converters. This method has been applied for partial CM voltage reduction [19], where two-level back-to-back inverters are synchronized at the same switching frequency, and zero-sequence injection is performed so that one inverter voltage pulse exactly coincides with one rectifier voltage pulse.

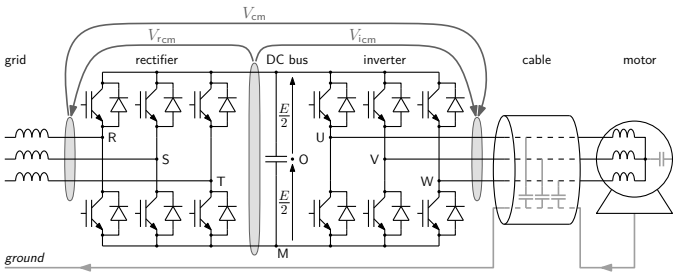


Fig. 1. Three-phase back-to-back inverters VSD with CM path to ground

This paper presents a new PWM strategy that theoretically provides full CM voltage cancellation for the whole converters association [21], [22]. Its major degrees of freedom are studied to demonstrate the limitations and opportunities using this method. Finally, experimental results are provided to validate the effectiveness of this strategy.

## II. Achieving CM Voltage Cancellation

### A. Basic Principle

In the following, the study is focused on a VSD system where the grid-connected inverter is referred to as the active

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front-end (AFE) rectifier. The CM voltage generated by a converter can be defined as the difference between the average of its output potentials and the average of its input potentials. Thus, according to Fig. 1, the CM voltage generated by the inverter can be defined as:

$$V_{\mathsf{icm}} = \frac{1}{3}\left(V_{\mathsf{UO}} + V_{\mathsf{VO}} + V_{\mathsf{WO}}\right), \tag{1}$$

and that generated by the rectifier is:

$$V_{\mathsf{rcm}} = \frac{1}{3}\left(V_{\mathsf{RO}} + V_{\mathsf{SO}} + V_{\mathsf{TO}}\right), \tag{2}$$

where O is the average DC bus potential. However, in some cases it is more convenient to use the lower DC potential (M) as a reference and to define CM voltages according to this point:

$$\begin{aligned} V_{\mathsf{icm}}^{\mathsf{M}} &= \tfrac{1}{3}\left(V_{\mathsf{UM}} + V_{\mathsf{VM}} + V_{\mathsf{WM}}\right) = V_{\mathsf{icm}} + \tfrac{E}{2} \\ V_{\mathsf{rcm}}^{\mathsf{M}} &= \tfrac{1}{3}\left(V_{\mathsf{RM}} + V_{\mathsf{SM}} + V_{\mathsf{TM}}\right) = V_{\mathsf{rcm}} + \tfrac{E}{2}, \end{aligned} \tag{3}$$

where $E$ is the DC bus voltage. The total CM voltage generated by both converters may be defined as:

$$V_{\mathsf{cm}} = V_{\mathsf{icm}} - V_{\mathsf{rcm}} = V_{\mathsf{icm}}^{\mathsf{M}} - V_{\mathsf{rcm}}^{\mathsf{M}} \tag{4}$$

In case the inverter and rectifier are synchronized at the same switching frequency, and controlled by conventional PWM strategy, Fig. 2 shows an example of switching patterns and both the individual and total CM voltages as defined in equations (1) to (4). Note that the inverter and rectifier pulses are arbitrarily ordered by decreasing width, though they could as well be positioned in any other order (different operating points) without changing the overall observations on the CM voltage: since each commutation of a single leg induces one CM voltage step, the resulting $V_{\mathsf{cm}}$ waveform naturally has 12 variations per switching period (6 legs with 2 commutations per leg per period). This voltage is responsible for bearing failures and its variations generate capacitive CM current circulating to the ground.

In order to reduce CM emissions, the CM voltage can be reduced by making two commutations happen at the same time so that their simultaneous contribution to CM voltage cancel each other. This is easily achieved by making one inverter voltage rise simultaneously with one rectifier voltage rise (the same would stand for voltage falls), as shown in Fig. 3. This can be realized by acting on the PWM intrinsic degrees of freedom.

### *B. Use of the PWM Degrees of Freedom*

In 2-level voltage-source converters, pulse-width modulation aims at building an arbitrary reference phase-to-DC-bus voltage ($V_{k\mathsf{M}}^*$ for phase $k$) by applying the DC voltage ($E$) during a fraction $\alpha_k$ (duty cycle) of the switching period ($T_{\mathsf{sw}}$), so that the average output voltage ($V_{k\mathsf{M}}$) equals its reference:

$$V_{k\mathsf{M}}^* = \langle V_{k\mathsf{M}} \rangle_{T_{\mathsf{sw}}} = \alpha_k E \quad \text{with} \quad 0 \leqslant \alpha_k \leqslant 1 \tag{5}$$

Since only the difference between two phase voltages of a given converter have to be controlled to feed the load, shifting all the phase references by the same amount of voltage (commonly called the zero-sequence component) is possible

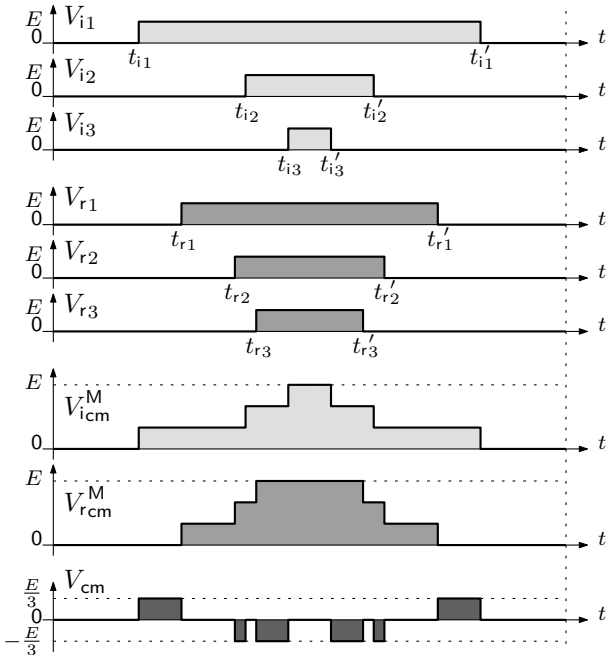


Fig. 2. Conventional PWM pattern and associated CM voltages for one switching period

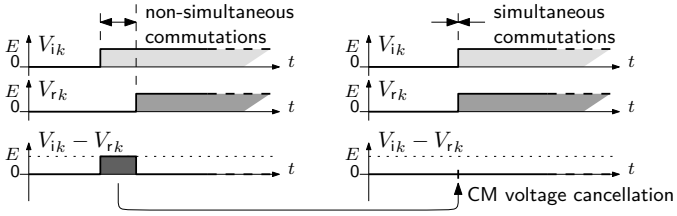


Fig. 3. Effect of inverter/rectifier switching synchronization on CM voltage

as long as all duty cycles remains in the $[0, 1]$ interval. Indeed, the zero-sequence voltage has no effect on the average phase-to-phase voltage and can thereby be freely used as a degree of freedom. It can be regarded as a reference voltage between the AC neutral point and the average DC potential (O), and is thereby expressed as:

$$V_0^* = \frac{1}{3}\sum_{k=1,2,3} V_{k\mathsf{O}}^* \tag{6}$$

Due to equations (1), (2) and (5), it is also the average value of the CM voltage generated by the considered converter.

In conventional sinus PWM, sinusoidal voltage references $V_{k\mathsf{O}}^*$ are centered around zero, which means that the zero-sequence voltage is null. Modifying its value results in changing the reference phase-to-DC-bus voltages:

$$\forall k \in \{1,2,3\}, \quad V_{k\mathsf{O}}^* = V_{k\mathsf{N}}^* + V_0^* \quad , \tag{7}$$

where $V_{k\mathsf{N}}^*$ are reference voltages between the phases and the AC neutral point. As a consequence, zero-sequence injection widens or narrows all the converter pulse widths by the same amount of time. In [19], this feature has been applied to the AFE/inverter association so as to equalize one rectifier pulse with one inverter pulse, thereby cancelling 4 CM voltage variations out of 12.

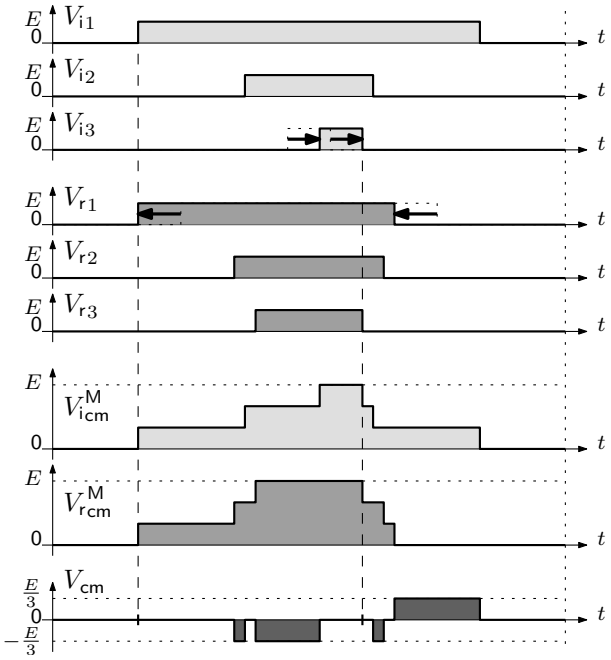


Fig. 4. Pulse positioning for the cancellation of some CM voltage variations

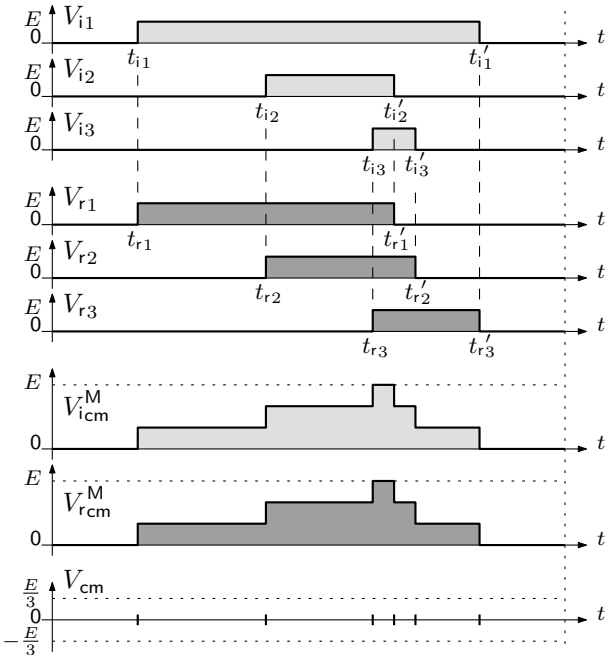


Fig. 5. PWM pattern example cancelling all CM voltage variations

Once the voltage references and the zero-sequence component are set, all six pulse widths of the VSDs are determined. Still, another degree of freedom is available as the pulses do not necessarily have to be stuck at the center of the switching period. Rather, they can be time-shifted inside the switching period while still satisfying equation (5). This pulse position can be used to move rectifier and inverter pulses so that their commutations coincide as shown in Fig. 4. Therefore, this possibility is yet another way to synchronize inverter and rectifier commutations.

The two aforementioned PWM degrees of freedom (zero-sequence component and pulse position) will be studied hereafter to derive a PWM method that completely eliminates the resulting CM voltage of the whole system.

## III. Proposed PWM strategy

### A. The Cyclic Pulse Sequencing

According to equation (4), full CM voltage cancellation is obtained when $V_{icm}^{M}$ and $V_{rcm}^{M}$ have exactly the same waveform at each switching period, which means that:

- the inverter and the rectifier operate at the same switching frequency and are synchronized
- each upward (rising) commutation of an inverter leg coincide with an upward commutation of a rectifier leg
- likewise, downward (falling) commutations coincide between one inverter and one rectifier leg

For that means, the PWM degrees of freedom must be used, especially regarding the position of the pulses inside the switching period. For all constraints to be met whatever the converters operating points, a cyclic association between inverter and rectifier voltage pulses is necessary, as explained hereafter.

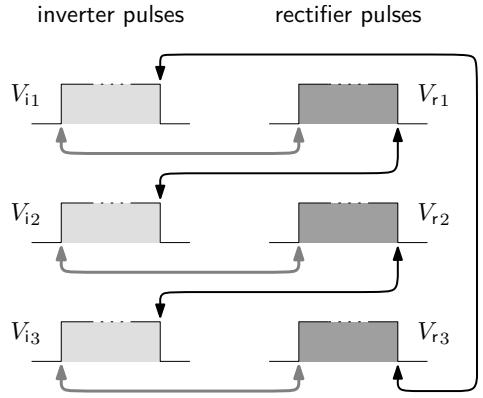


Fig. 6. Cyclic sequencing of pulses to achieve CM voltage elimination

Figure 5 presents such an association, where the rising and falling commutations of any pulse are always synchronized with commutations in the same direction in the other converter (for convenience, notation $V_{i_k}$ stands for the $k^{\text{th}}$ inverter $V_{k\text{M}}$ voltage, and $V_{r_k}$ likewise for the rectifier). As a consequence, $V_{icm}^{M}$ equals $V_{rcm}^{M}$ and the resulting $V_{cm}$ voltage is kept null during the whole switching period. In order to avoid special cases that may not happen in the general case (such as equal pulse widths of inverter and rectifier legs), it can be noted that the commutations of one converter leg are always synchronized with commutations of two different legs in the other converter. This leads to a cyclic sequence in the way commutations are synchronized, as summarized in Fig. 6: the first inverter upward commutation (on $V_{i1}$) is synchronized with the first rectifier one (on $V_{r1}$), then the downward commutation of this leg is synchronized with that of a second inverter leg ($V_{i2}$), and so on, until the last rectifier downward commutation (on $V_{r3}$) is synchronized with that of $V_{i1}$.

It is noteworthy that the feasibility of such pulse association

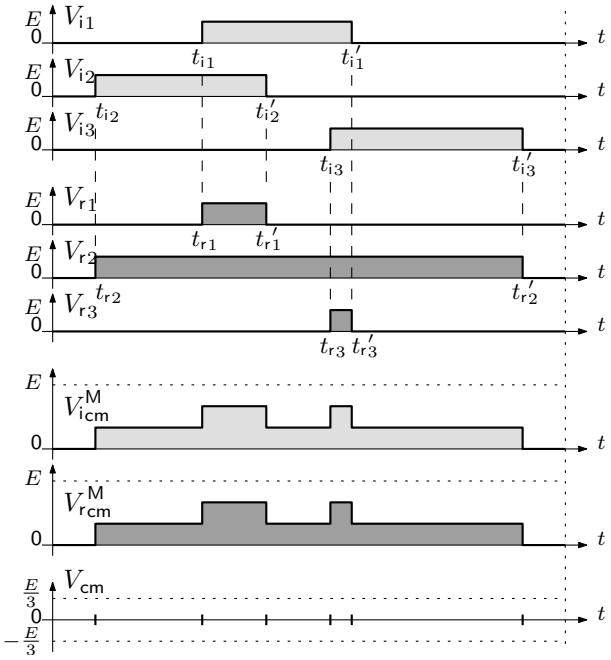


Fig. 7. PWM pattern example applied to another operating point

is not dependant on the converters operating points nor related to any specific sector of the vector diagram. For instance, Fig. 7 presents the same association pattern as Fig. 5 in case the inverter operates with low output voltage (the three inverter pulses have about the same width, which could correspond to low motor speed) while the rectifier operates at high modulation index (both large and small pulses involved, indicating high phase-to-phase voltages). Furthermore, the sectors are changed since the largest pulses are now on the third leg for the inverter and the second for the rectifier. It can be verified that the $V_{\mathsf{icm}}$ and $V_{\mathsf{rcm}}$ voltages still have the same waveforms, resulting in zero $V_{\mathsf{cm}}$ voltage.

Actually, the cyclic sequence is always effective regardless the individual pulse widths as long as a specific constraint is respected on the zero-sequence voltage. This constraint is detailed in the next section. It should also be noted that the inverter U, V, W and rectifier R, S, T phases can be substituted to the 1, 2, 3 indexes in any order: this degree of freedom will be discussed in section III-C.

### *B. Contraints Related to the Zero-Sequence Component*

According to Fig. 5, with $(t_{\mathsf{i}k}\,;\,t_{\mathsf{i}k}')$ respectively the rise and fall instants of the $k^{\text{th}}$ inverter leg, and $(t_{\mathsf{r}k}\,;\,t_{\mathsf{r}k}')$ those of the $k^{\text{th}}$ rectifer leg, the following conditions should be satisfied:

$$\begin{array}{lll} t_{\mathsf{i}1} = t_{\mathsf{r}1} & & t_{\mathsf{r}1}' = t_{\mathsf{i}2}' \\ t_{\mathsf{i}2} = t_{\mathsf{r}2} & & t_{\mathsf{r}2}' = t_{\mathsf{i}3}' \\ t_{\mathsf{i}3} = t_{\mathsf{r}3} & & t_{\mathsf{r}3}' = t_{\mathsf{i}1}' \end{array} \quad . \tag{8}$$

Thus, the widths $T_{\mathsf{i}k}$ and $T_{\mathsf{r}k}$ of the inverter and rectifier pulses verify:

$$\begin{aligned} \sum_{k=1,2,3} T_{\mathsf{i}k} &= (t_{\mathsf{i}1}' - t_{\mathsf{i}1}) + (t_{\mathsf{i}2}' - t_{\mathsf{i}2}) + (t_{\mathsf{i}3}' - t_{\mathsf{i}3}) \\ &= t_{\mathsf{r}3}' + \underbrace{(-t_{\mathsf{r}1} + t_{\mathsf{r}1}')}_{T_{\mathsf{r}_1}} + \underbrace{(-t_{\mathsf{r}2} + t_{\mathsf{r}2}')}_{T_{\mathsf{r}_2}} - t_{\mathsf{r}3} \\ &= \sum_{k=1,2,3} T_{\mathsf{r}k} \end{aligned} \tag{9}$$

Therefore, complete cancellation of the total CM voltage can always be achieved as long as the sum of the inverter pulse widths equals the sum of the rectifier ones. Indeed, starting from the $V_{\mathsf{i}1}$ rising edge in Fig. 6, each new synchronization involves a new pulse and thereby can always be realized until the final ($6^{\text{th}}$) one, where the very last rectifier falling edge (on $V_{\mathsf{r}3}$) must exactly coincide with the very first inverter one (on $V_{\mathsf{i}1}$). Traveling this cycle by counting positively the rectifier pulse widths and negatively the inverter ones, it appears that this remaining synchronization is guaranteed when the sums of pulse widths are equal. This condition can be transposed as an equality between the sum of inverter and rectifier duty cycles, and thereby between the sum of the reference phase-to-DC-bus voltages according to equation (5):

$$\sum_{k=1,2,3} V_{\mathsf{i}k}^{*} = \sum_{k=1,2,3} V_{\mathsf{r}k}^{*} \quad , \tag{10}$$

which means that zero-sequence components of the inverter and rectifier should be equal in the considered AFE/inverter association. Fig. 8 presents an example of such zero-sequence addition that widens all rectifier and inverter pulses by the same amount, preserving the sum-of-widths equality and still achieving CM voltage cancellation. In contrast, Fig. 9 shows the result of the same cyclic association when the sum-of-widths is different (unequal zero-sequence on inverter and rectifier): two commutations remain unmatching and the end of the cycle, leading to a non-cancelled CM voltage pulse.

As a drawback, this zero-sequence-equality constraint prevents free use of this degree of freedom on each converter separately. This parameter usually allows to increase the conversion ratio between AC voltages and the DC bus voltage [23], so that the amplitude of the reference voltages between one phase and the AC neutral point ($\widehat{V_{k\mathsf{N}}^{*}}$) can be increased above $\frac{E}{2}$ (linear voltage extension up to $\frac{E}{\sqrt{3}}$), while keeping phase-to-DC-bus voltages $V_{k\mathsf{O}}^{*}$ below the $\frac{E}{2}$ physical limit. Figure 10 shows an example of such zero-sequence injection on the inverter side when $\widehat{V_{k\mathsf{N}}^{*}}$ is equal to $1.1 \times \frac{E}{2}$. Actually, the equality constraint on zero-sequence components implies that any voltage extension in a given converter must be compensated by a similar decrease of the conversion ratio in the other converter (at least in the general case where motor and grid voltages are not synchronous). Figure 10 shows this limitation on the rectifier part because the zero-sequence voltage has been chosen for the inverter side and is not adapted to the rectifier reference voltages.

Thus, the limitations for input and output voltages are depicted in Fig. 11, where the example of Fig. 10 is identified as point "A". If no DC voltage boost is required, then the

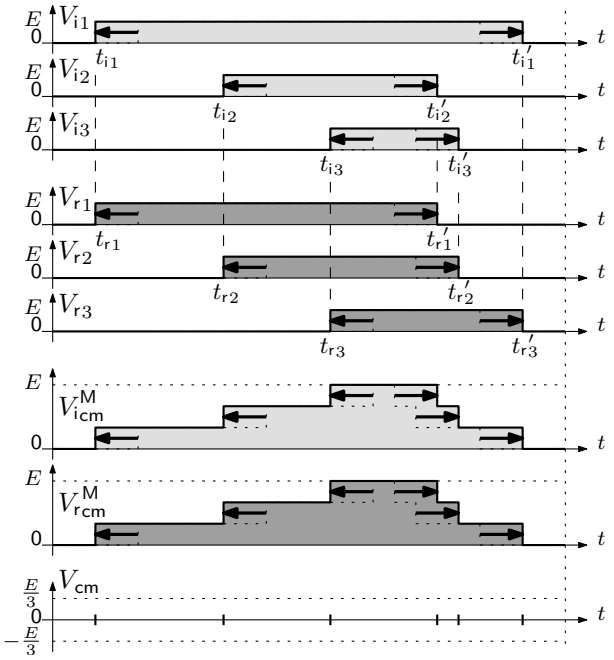


Fig. 8. PWM pattern from Fig. 5 with equal zero sequence injection on both converters

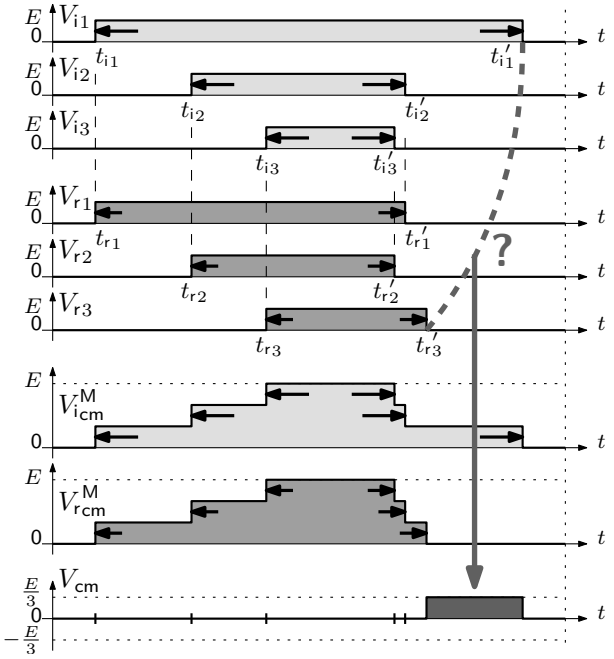


Fig. 9. PWM pattern from Fig. 5 with unequal zero sequence injection

DC bus voltage is typically controlled to be as small as possible; therefore, the rectifier conversion ratio and thereby the reference phase-to-AC-neutral voltages should be as high as possible. However, in the worst situation when inverter and rectifier AC voltages have the same amplitude, then linear voltage extension is not possible and $V_0^*$ should remain null. Compared with conventional PWM strategies where voltage extension could be performed on both converters, this results in a larger DC bus voltage by a factor of $\frac{2}{\sqrt{3}}$, which is about 15% higher and should be taken into account in the converters

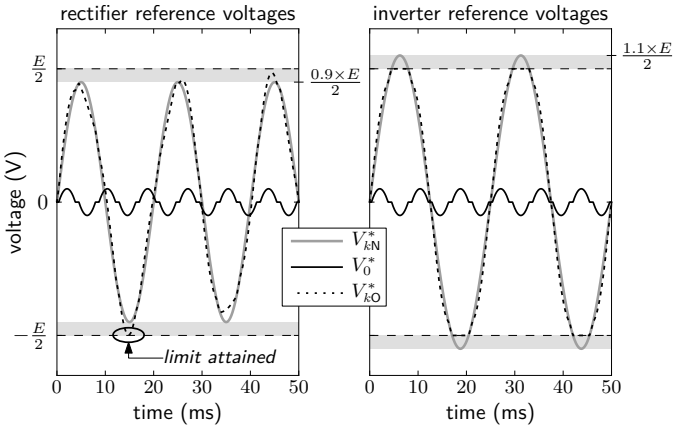


Fig. 10. Zero-sequence injection for inverter voltage extension applied to the rectifier as well

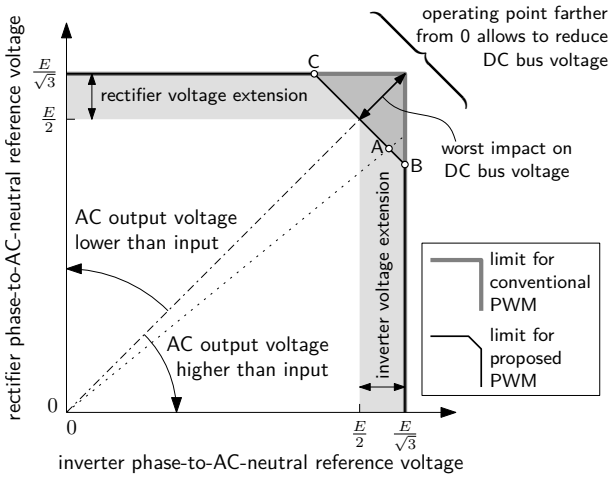


Fig. 11. Comparison of zero-sequence injection possibilities for linear voltage extension using different PWM strategies

design. However, any input-to-output transfer ratio can still be obtained, and the aforementioned oversizing disappears when the output AC voltages are either higher than $\frac{1}{\sqrt{3}-1} \approx 1.366$ times the input ones (starting from point "B" and below) or lower than $\sqrt{3}-1 \approx 0.732$ times the input voltages (left of point "C").

### C. Multiplicity of the Possible Pulses Associations

The synchronization solution presented in Fig. 5 is not the only possibility to cancel all CM voltage variations. For instance, Fig. 12 presents other ways to synchronize all commutations in the same operating point (inverter and rectifier pulse widths). Indeed, several combinations exist depending on how the actual R, S, T and U, V, W legs are tied to the 1, 2, 3 indexes.

Once zero-sequence components are set equally for the two converters, the number of possible pulses associations can be determined based on Fig. 6, taking arbitrarily the inverter phase U as a starting point:

- its rising edge should be synchronized with the rising edge of either R, S, or T rectifier leg (3 choices)

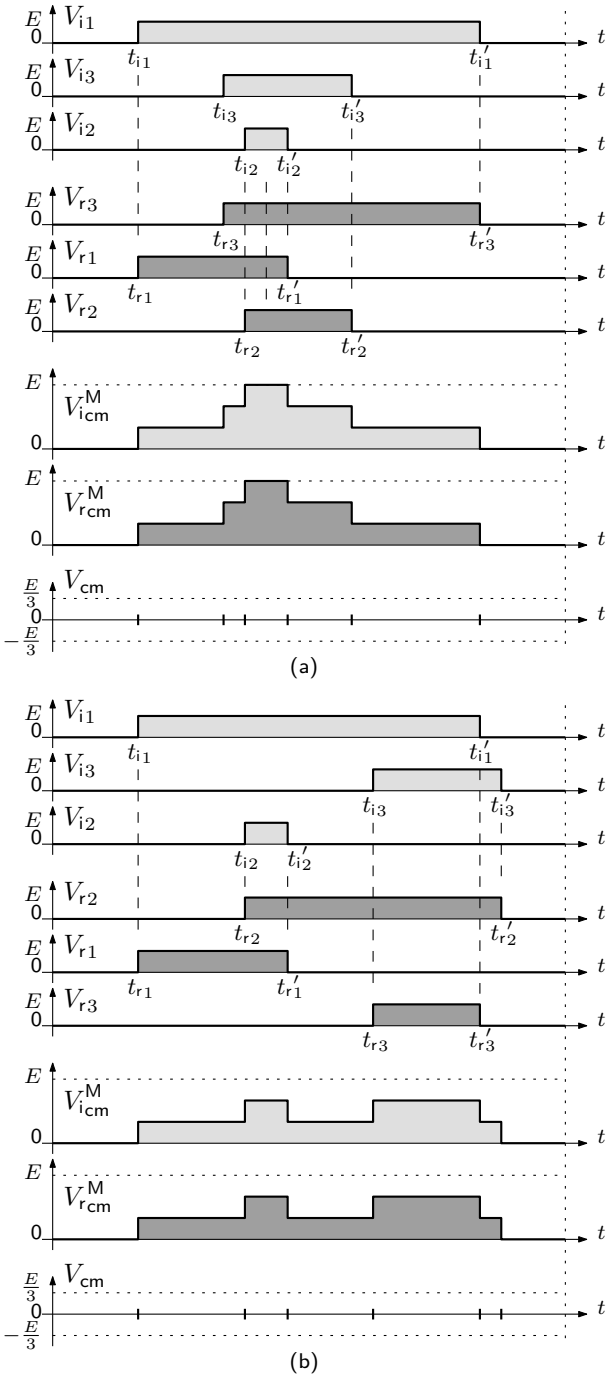


Fig. 12. Alternative PWM patterns cancelling all CM voltage variations

- having selected one of them, say R for instance, its falling edge should be synchronized with one falling edge among the two remaining inverter legs (V or W) (2 choices)
- assuming for example that leg V is selected, then its rising edge should be synchronized with a rising edge among the two remaining rectifier legs (for instance, S or T in this case) (2 choices)
- no more choices are necessary since the falling edge of this rectifier leg (say, S) has to coincide with that of the last inverter leg (W), of which the rising edge must coincide with that of the last remaining rectifier leg (T), of which the falling edge will naturally coincide with the falling edge of the initial inverter leg (U).

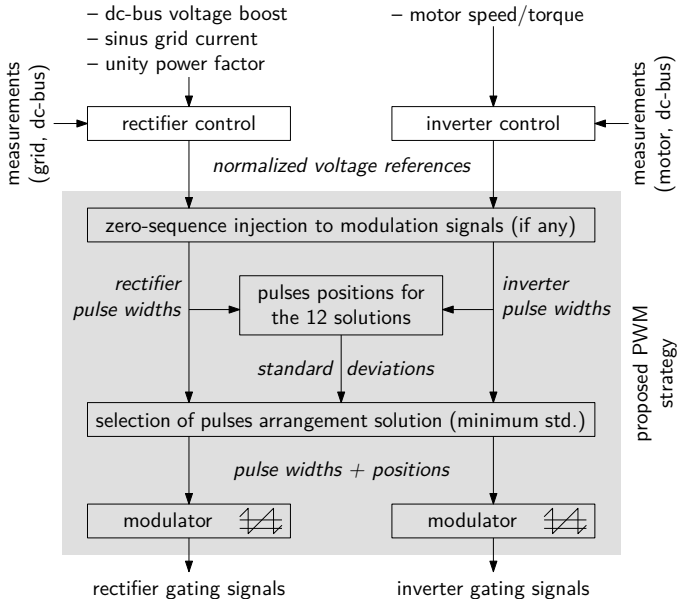


Fig. 13. Implementation overview of the proposed method

Thus, there are in total 12 different possible choices ($3 \times 2 \times 2$) to perform a cyclic sequence that synchronizes all commutations of both converters. One possible formalism to identify these choices consists in naming the 3 selected legs in the 3 first steps above that involve a choice. In other words, the naming convention determines the physical legs associated with $V_{r1}$, $V_{i2}$, and $V_{r2}$ respectively. For instance in the given example, the selected choice could be named "RVS". Likewise, the 12 possible solutions can be determined as: RVS, RVT, RWS, RWT, SVR, SVT, SWR, SWT, TVR, TVS, TWR, TWS. In order to choose from these possibilities, one simple implementation consists in avoiding situations like Fig. 12b where pulses are positioned far from each other, much different from the nesting effect obtained with conventional PWM strategies (Fig. 2). This could be achieved by selecting a synchronization solution that minimizes the standard deviation of the pulses positions. Indeed, grouping pulses as much as possible like in Fig. 12a is a good option to avoid degrading too much the current ripple in the AC line inductors or in motor windings. It is also possible to focus on the pulses of a given converter, for instance favouring the rectifier to prevent oversizing of the grid-side inductors. Thus, a possible implementation of the proposed PWM strategy is depicted in Fig. 13: once pulse widths are set in accordance with the instantaneous voltage references, the relative pulse positions (e.g. their center instant) can be determined for the 12 solutions so as to select the most grouping one. Note that the subsequent "modulator" part is detailed in section IV-B. The following section shows the effect of the proposed method on the quality of output voltages.

### D. Impact on output voltages

Since the proposed PWM strategy modifies the pulses positions compared with conventional methods, a degradation of AC voltage quality can be expected. Figure 14 presents simulation waveforms when the rectifier operates at 50 Hz fundamental frequency and boosts the 230 V AC mains to a 540 V DC bus (modulation index is 0.7) while the inverter operates at 20 Hz and produces a 152 V phase-to-phase voltage (modulation index is 0.46). The VSD supplies a 11 kW induction motor (380 V, 50 Hz nominal) at full load with constant voltage/frequency ratio. The switching frequency is 4 kHz. Phase-to-phase voltages are plotted as well as line currents and both the individual and total CM voltages. Input power factor correction can be verified as the line current (Fig. 14c) is in phase with the mains voltage of the same line (Fig. 14a). The first part (until 50 ms) is obtained with a conventional PWM strategy. The phase-to-phase voltages exhibit typical positive and negative half waves where the reference voltage is synthesized by modulating between the two nearest voltage levels $\{0, +E\}$ or $\{0, -E\}$. At time 50 ms, the modulation method is suddenly changed to the proposed PWM with pulses grouping (Fig. 13). As a consequence, the total CM voltage becomes zero starting from this time in Fig. 14g (assuming ideal commutations and thereby perfect cancellation). However, the phase-to-phase voltages are sometimes modulated using all three voltage levels $\{-E, 0, +E\}$, which is not as good as with the conventional strategy. The actual shape of the voltage pulses including 2- and 3-level modulation can be seen more clearly in the enlarged view over 16 switching periods in Fig. 15. It is noteworthy that places where 3-level modulation happen are only a consequence of non-nested phase-to-DC-bus voltages (Fig. 15a and d), and that the resulting average value still satisfies the voltage reference requirements. CM voltages are also more distinguishable, showing that the individual $V_{\mathsf{rcm}}$ and $V_{\mathsf{icm}}$ waveforms vary identically, resulting in zero $V_{\mathsf{cm}}$ voltage.

Harmonic performance can be quantified by the total harmonic distortion (THD) defined in eq. (11), where $U_k$ is the magnitude of the $k^{\text{th}}$ harmonic, which takes into account all harmonics with equal importance:

$$\text{THD} = \frac{\sqrt{\sum_{k\geqslant 2} {U_k}^2}}{U_1} \quad ; \quad \text{DF} = \frac{\sqrt{\sum_{k\geqslant 2} \left(\frac{U_k}{k}\right)^2}}{U_1}. \qquad (11)$$

The weighted distortion factor (DF) can also be determined to give a better representation of low-order harmonics that will eventually be reflected in the line currents. These quantities are computed over one fundamental period of either converter. Since the common period for both converters is larger (100 ms in the simulation example for 20 ms rectifier and 50 ms inverter periods), their value may also depend on the relative phase shift between the rectifier and inverter reference voltages. It is also a function of the modulation depth. THD and DF values of the phase-to-phase rectifier and inverter voltages with various phase shifts have been computed up to 100 kHz and reported in Table I for three different inverter voltages (modulation index in the first line of the table) and for three different PWM strategies each time:

TABLE I
HARMONIC PERFORMANCE OF RECTIFIER AND INVERTER PHASE-TO-PHASE VOLTAGES WITH DIFFERENT MODULATION STRATEGIES

| modulation index | | | 0,3 | | | 0,6 | | | 0,9 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PWM strategy | | | A | B | C | A | B | C | A | B | C |
| what | where | phase shift (deg) | % | % | % | % | % | % | % | % | % |
| THD | rectifier | 0 | 103 | 106 | 146 | 103 | 107 | 157 | 103 | 132 | 157 |
| | | 90 | 103 | 106 | 145 | 103 | 108 | 157 | 103 | 133 | 158 |
| | | 180 | 103 | 107 | 146 | 103 | 108 | 157 | 103 | 134 | 160 |
| | | 270 | 103 | 107 | 147 | 103 | 108 | 157 | 103 | 133 | 159 |
| | inverter | 0 | 191 | 319 | 390 | 118 | 139 | 189 | 78 | 80 | 106 |
| | | 90 | 191 | 322 | 390 | 118 | 139 | 191 | 78 | 79 | 108 |
| | | 180 | 192 | 321 | 390 | 118 | 138 | 195 | 78 | 80 | 107 |
| | | 270 | 191 | 322 | 390 | 118 | 139 | 188 | 78 | 81 | 106 |
| DF | rectifier | 0 | 0,67 | 0,75 | 1,67 | 0,67 | 0,99 | 1,72 | 0,67 | 1,51 | 1,80 |
| | | 90 | 0,67 | 0,76 | 1,69 | 0,67 | 0,98 | 2,03 | 0,67 | 1,39 | 1,83 |
| | | 180 | 0,67 | 0,81 | 1,48 | 0,67 | 1,00 | 2,07 | 0,67 | 1,53 | 1,84 |
| | | 270 | 0,67 | 0,76 | 1,67 | 0,67 | 0,93 | 1,72 | 0,67 | 1,53 | 1,78 |
| | inverter | 0 | 0,30 | 1,11 | 1,51 | 0,43 | 0,82 | 1,34 | 0,56 | 0,68 | 1,14 |
| | | 90 | 0,28 | 1,08 | 1,45 | 0,44 | 0,85 | 1,38 | 0,56 | 0,66 | 1,06 |
| | | 180 | 0,31 | 1,09 | 1,42 | 0,44 | 0,84 | 1,41 | 0,55 | 0,67 | 1,10 |
| | | 270 | 0,29 | 1,12 | 1,49 | 0,43 | 0,86 | 1,33 | 0,55 | 0,67 | 1,12 |

"A" is the conventional one, "B" is the proposed method with pulses grouping, and "C" without grouping. First, it appears that the inverter/rectifier phase shift does influence much the resulting percentages. Second, as expected, it appears that the proposed PWM increases the harmonic content compared with a conventional strategy. However, the DF is kept small which indicates that the high THD values are due to high frequency components rather that low-order ones. Confirmation of this behavior can be obtained by frequency-domain analysis of the phase-to-phase voltage waveforms from Fig. 14, which is shown in Fig. 16: the new strategy mainly involves larger harmonic families around multiple times the switching frequency. Finally, comparing strategies "B" and "C" in Table I also reveals that the pulses grouping criteria is effective in limiting the harmonic degradation due to pulses positioning.

Note that apart from output voltages quality, another interesting criteria that may be impacted by the pulses positioning is current that flows in the DC-bus capacitor, which is chopped at the switching frequency. An RMS value of 10.5 A has been computed with the conventional strategy in the simulation conditions of Fig. 14. Due to non-optimal pulses positions, the proposed PWM slightly increases this value at 12.7 A. Again, the pulse grouping is effective regarding this criteria as the RMS current would rise above 20 A otherwise. Again, these figures validate the interest of the pulses-grouping implementation depicted in Fig. 13.

## IV. Experimental Results

### A. Measurement Setup

The proposed PWM strategy has been implemented in an experimental setup (Fig. 17) including two 15 kW-rated back-to-back inverters switching at 4 kHz and a development control board based on DSPs. The dead time is set to 2 µs. A shielded, 4-wire, 25-meter cable is used to connect the VSD to a 11 kW induction machine of 380 V, 50 Hz nominal voltage. The 230 V mains are rectified to a 530 V DC bus from which the inverter supplies the motor at 150 V, 20 Hz in these tests.

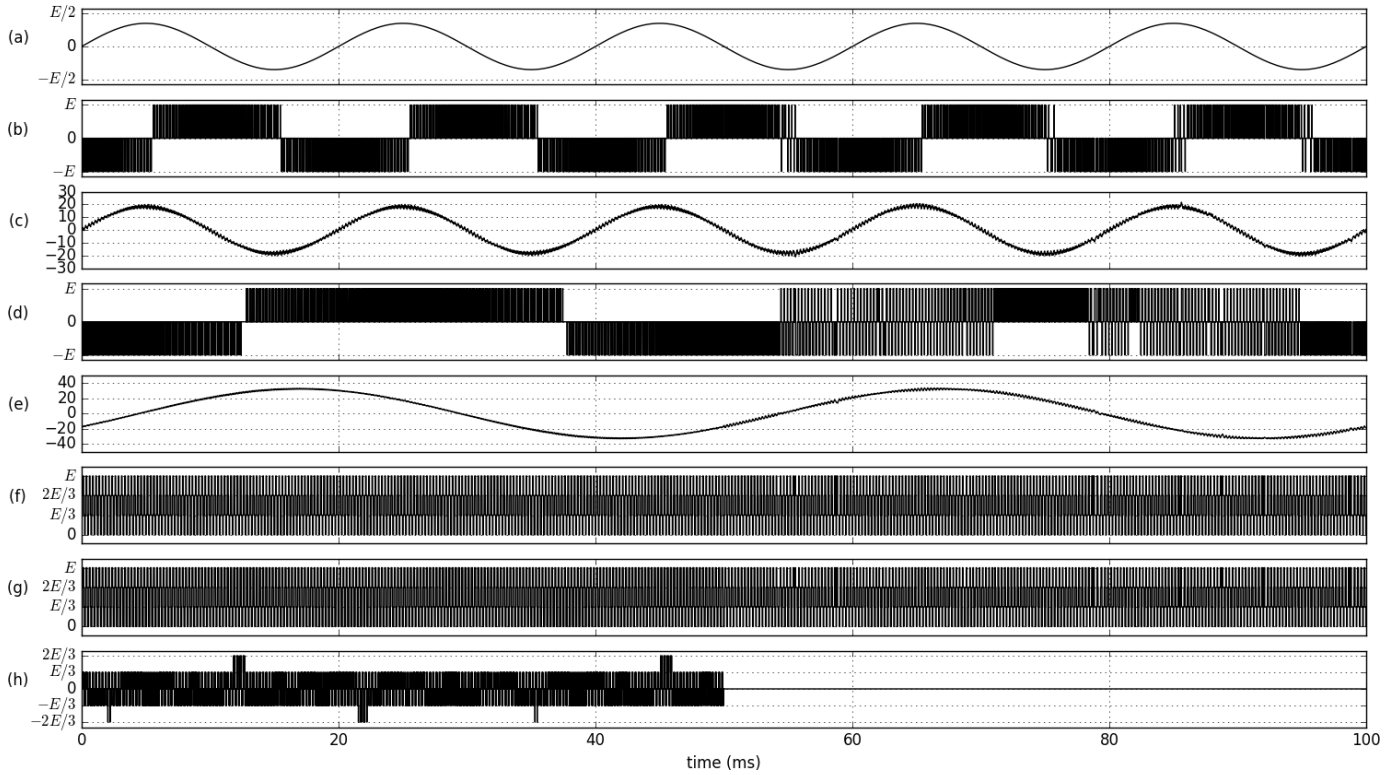


Fig. 14. VSD time-domain waveforms comparison between conventional (before 50 ms) and proposed (after 50 ms) PWM strategy. (a) grid phase-R-to-neutral voltage; (b) $U_{\mathsf{ST}}$ rectifier phase-to-phase voltage; (c) rectifier R-line current (A); (d) $U_{\mathsf{VW}}$ inverter phase-to-phase voltage; (e) inverter U-line current (A); (f) $V_{\mathsf{rcm}}$ rectifier CM voltage; (g) $V_{\mathsf{icm}}$ inverter CM voltage; and (h) $V_{\mathsf{cm}}$ total CM voltage

TABLE II
KIND OF SWITCHING TO DETERMINE THE NEED FOR DEAD-TIME COMPENSATION

| | current flows out toward AC | current flows in toward DC |
|---|---|---|
| voltage rises | diode-to-transistor → *dead time* | transistor-to-diode |
| voltage falls | transistor-to-diode | diode-to-transistor → *dead time* |

Dead-time effects are known to reduce the effectiveness of simultaneous switching for CM voltage reduction [12], [24]. Therefore, the proposed PWM strategy has been tested both with and without a conventional dead-time compensation method based on the measured direction of input and output phase currents [25]. Basically, turn-on (diode-to-transistor) commutations are identified so that their logical signals are time-shifted by the dead-time value for the actual voltage transition to occur at the expected instant. Table II summarizes commutations in which dead times are involved depending on the current sign and the phase-to-DC-bus voltage variation. Finally, a conventional sinus PWM (SPWM) strategy has also been tested for comparison purposes of the drive EMC performance.

### B. Carrier-based implementation

Once the control algorithm has determined the pulse association cycle, modulation signals can be sent to the modulator. The proposed method requires microcontroller PWM peripherals that allow to freely position pulses within the switching period. In this experimental setup, the TI TMS320F28335 DSC has been used. Instead of generating a pulse by comparing only one modulation signal with the carrier wave (Fig. 18a), it can be configured to compare two modulation signals with a saw-tooth carrier, and to define the actions at the crossing instants so that the first modulation signal ($m_1$) determines the start of the pulse (upward commutation) while the second one ($m_2$) determines its end (downward commutation) as shown in Fig. 18b. Thus, pulse width can be controlled by their difference $\Delta m$ and its position can be controlled by $m_1$, which is a convenient capability for the implementation of the proposed method.

### C. Time and Frequency Domain Results

The measured individual motor-side and grid-side CM voltages (respectively, $V_{\mathsf{icm}}$ and $V_{\mathsf{rcm}}$ in Fig. 1) are presented in Fig. 19 along with the resulting total CM voltage ($V_{\mathsf{cm}}$) during 5 switching periods. While the conventional strategy generates 12 CM voltage steps per switching period (Fig. 19c), the proposed PWM strategy cancels the total CM voltage (Fig. 19f) by achieving identical rectifier and inverter individual CM voltage waveforms (Fig. 19d and e). Meanwhile, voltage references are still satisfied and control functionalities such as unity input power factor are kept; indeed, Fig. 20 shows that the overall input current is not affected by the proposed method. This current actually has some harmonics (11.6 % and 12.0 % THD, respectively, with 2.22 % and 2.30 % DF), which is possibly

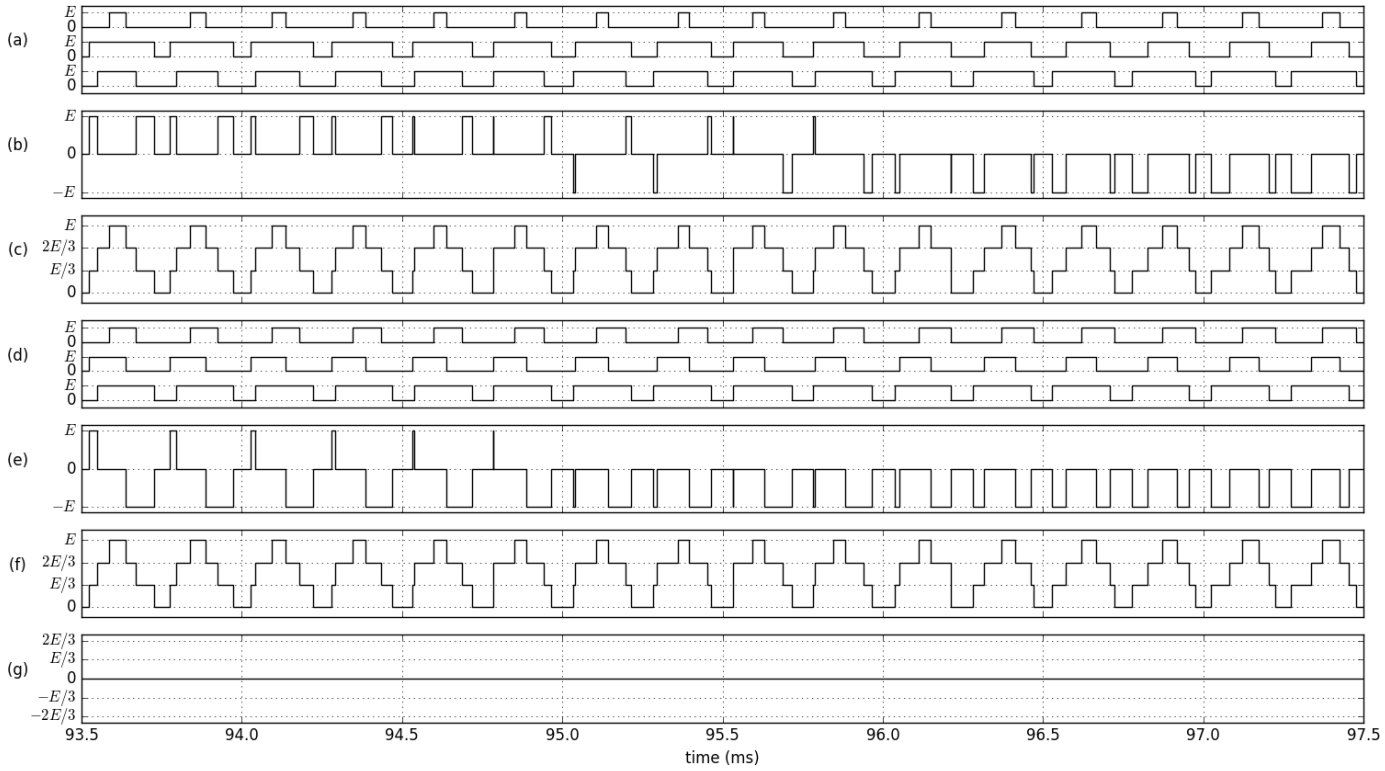


Fig. 15. Enlarged view of time-domain voltage waveforms from Fig. 14 during application of the proposed PWM method. (a) $V_{\mathsf{RM}}$, $V_{\mathsf{SM}}$, and $V_{\mathsf{TM}}$ rectifier phase-to-DC-bus voltages; (b) $U_{\mathsf{ST}}$ rectifier phase-to-phase voltage; (c) $V_{\mathsf{rcm}}$ rectifier CM voltage; (d) $V_{\mathsf{UM}}$, $V_{\mathsf{VM}}$, and $V_{\mathsf{WM}}$ inverter phase-to-DC-bus voltages; (e) $U_{\mathsf{VW}}$ inverter phase-to-phase voltage; (f) $V_{\mathsf{icm}}$ inverter CM voltage; and (g) $V_{\mathsf{cm}}$ total CM voltage

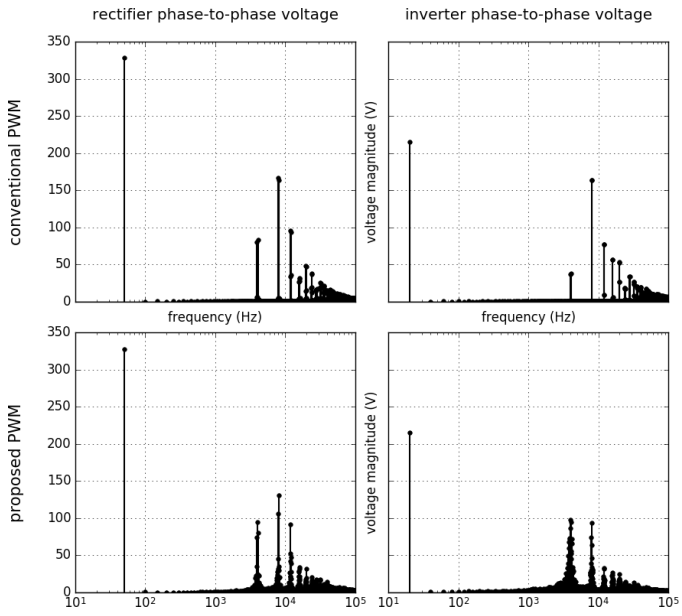


Fig. 16. Rectifier and inverter phase-to-phase voltage spectra

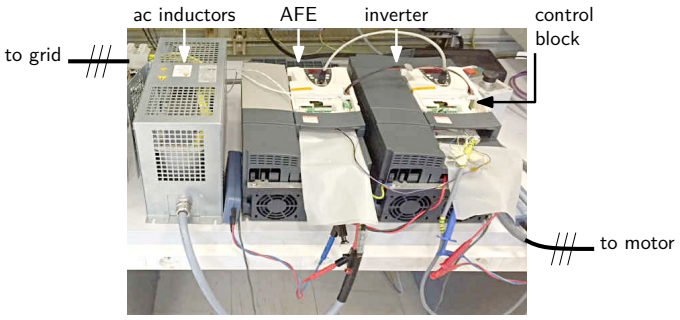


Fig. 17. The experimental test bench

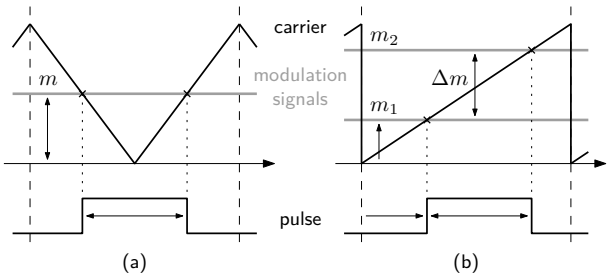


Fig. 18. Pulse-width modulators (a) typical; (b) used for implementation

due to the simplicity of the implemented AFE control loop that may not be able to compensate for the small unbalance and distortion of the practical three-phase network.

The preceding results where actually obtained using dead-time compensation as mentioned in section IV-A. In order to evaluate its effect, Fig. 21 presents the total measured CM voltage between motor-side and grid-side potentials during only one switching period. In the medium curve, it can be seen that the proposed method without dead-times compensation cancels the CM voltage except for thin pulses of the width

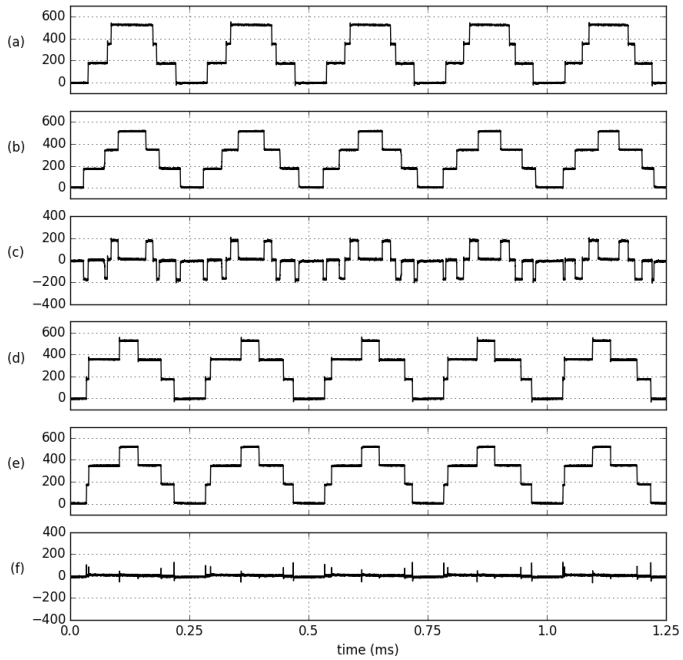


Fig. 19. Measured CM voltage waveforms with (a–c) the conventional PWM strategy: (a) $V_{\mathsf{icm}}$ inverter (V); (b) $V_{\mathsf{rcm}}$ rectifier (V); (c) $V_{\mathsf{cm}}$ total (V); and (d–f) with the proposed PWM method: (d) $V_{\mathsf{icm}}$ inverter (V); (e) $V_{\mathsf{rcm}}$ rectifier (V); and (f) $V_{\mathsf{cm}}$ total (V)

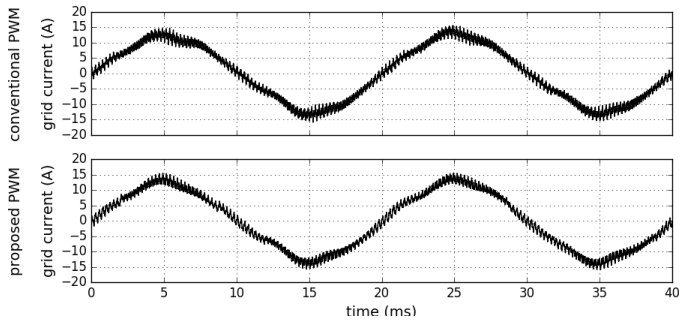


Fig. 20. Measured grid current with both PWM strategies

of the dead time. These pulses are then suppressed using the dead-time compensation, resulting in a flat CM voltage in which some residual spikes remain at the commutations instants. This can be explained by the simultaneous switching waveforms that may not have the exact same $dv/dt$. Indeed, the voltage waveform may be influenced by the commutation kind (Table II) and the value of the phase current and temperature [26], resulting in non-perfect CM voltage cancellation during the commutation process [27]. Still, the proposed PWM significantly reduces the CM voltage, so that in VSD applications, the converter operation should become safe for motor bearings.

Furthermore, Fig. 22 presents the frequency-domain spectra of the CM voltage, obtained by performing FFT on the time-domain waveforms over the fundamental system period. Post-processed envelopes are also plotted to facilitate comparisons. This experimental result confirms the relevance of dead-time compensation and shows that the proposed strategy reduces CM voltage by more than $15\,\mathrm{dB}$ at switching frequency and

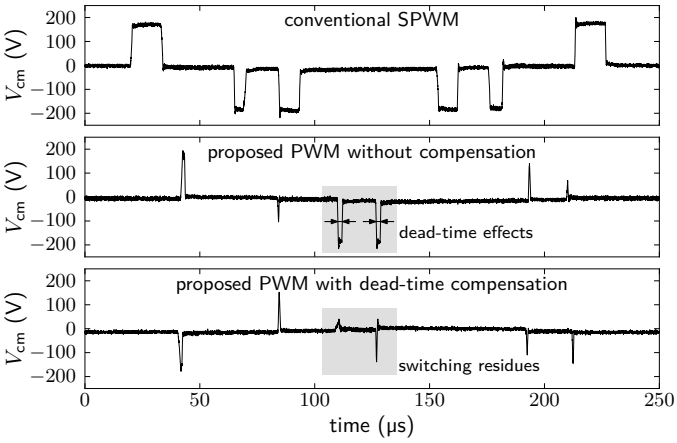


Fig. 21. Measured CM voltage waveform during one switching period

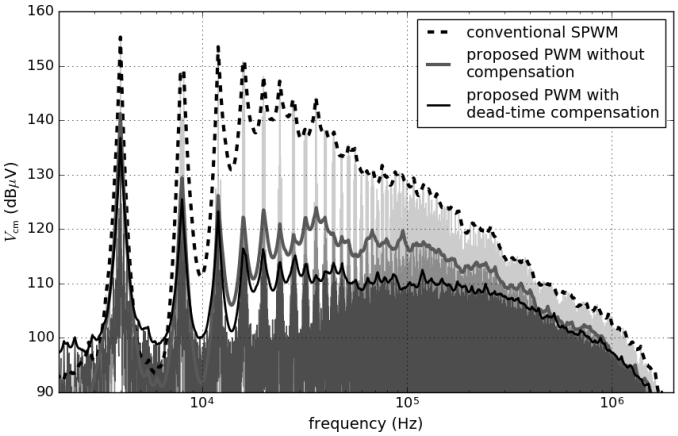


Fig. 22. Frequency-domain spectrum of measured CM voltage

at $150\,\mathrm{kHz}$, which is the starting point for the regulation of high-frequency conducted emissions in most standards such as IEC-61800-3. These values are especially important for VSD input EMI filters design, and show that a reduction of the filter volume can be expected using the proposed method.

## V. Conclusion

A new PWM strategy is presented for the reduction of common-mode voltage generated by 3-phase back-to-back two-level voltage-source inverters used in variable-speed motor drive applications. This strategy theoretically cancels all CM voltage transitions of the whole converters association whatever its operating point, thereby allowing a better EMC behavior on both motor side (no bearing failure) and grid side (smaller EMI filter). The degrees of freedom of this strategy on zero-sequence component and cyclic pulse sequencing are studied, and an experimental implementation is performed to validate its effectiveness. It is shown that dead-time effect should be compensated to optimize EMC performance, and that more than $15\,\mathrm{dB}$ reduction is obtained from the switching frequency up to a few hundred kilohertz. Future work should focus on the PWM strategy impact on the design of the grid-side EMI filter, which requires careful identification of CM currents propagation paths. Differential-mode power quality

should also be analyzed to assess the possible trade-offs with common-mode performance when using the proposed PWM strategy.

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