Characterization Method of SiC-JFET Interelectrode Capacitances in Linear Region

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***Abstract*—In order to study switching waveforms of a SiC-JFET, its inter-electrode capacitances evolution is necessary when the power device is in linear region. In this paper, the reverse transfer capacitance $C_{\rm gd}$ is at first characterized by the multiple-current-probe method and afterwards validated by the measurement with an impedance analyzer. The output capacitance $C_{\rm oss}$ is measured by the same method and compared with the single-pulse characterization, which shows a huge increase of the apparent capacitance values in linear region. The influence of the power transistor internal gate resistor is thus studied, revealing the inter-electrode capacitances measurement difficulties when the power device is in linear region. The characterization results are allowed to finely model the power transistor of which the switching behaviors are validated with the measurement in a buck converter.**

***Index Terms*—SiC-JFET; Inter-electrode capacitances; Linear region; Multi-current-probe method; single-pulse characterization; Gate resistance $R_{\rm g}$**

I. INTRODUCTION

WIDE bandgap power semi-conductor devices are playing an important role in the future energy conversion system development [1]–[3] [4], thus it is necessary to know well their characteristics to optimize their use for high-temperature, high-efficiency and high-frequency power converters design [5]–[8]. Power semi-conductor devices characteristics can be divided on static characteristics and dynamic characteristics, of which the latter is mainly represented by their inter-electrode capacitances non-linear evolution on different power device electrical parameters. When the power transistor is in OFF-state, the influence of both $V_{\rm DS}$ and $V_{\rm GS}$ voltages on inter-electrode capacitances is presented by authors in [9]–[11] for the case of a Si-MOSFET, a SiC-MOSFET and a SiC-JFET respectively. The determination of these capacitances values in high blocking $V_{\rm DS}$ voltage plays an important role to determine the resonance frequency at the end of the transistor turn-off switching, thus to determine the electromagnetic interference (EMI) level induced by the power converter [12].

It is presented in Fig. 1 a power transistor switching mesh and the ideal $I_{\rm D}$ switching current, $V_{\rm DS}$ and $V_{\rm GS}$ switching voltage waveforms, in which it is shown that during $V_{\rm DS}$ switching, $V_{\rm GS}$ is superior to the threshold voltage $V_{\rm th}$ and there is current in the power transistor channel. In order to propose a fine power transistor model, it is necessary to know well the influence of $I_{\rm D}$ or $V_{\rm GS}$ and $V_{\rm DS}$ voltages on inter-electrode capacitances values. The influence of the switching current on inter-electrode capacitances evolution is presented by authors in [13], [14] in the case of a Si-MOSFET.

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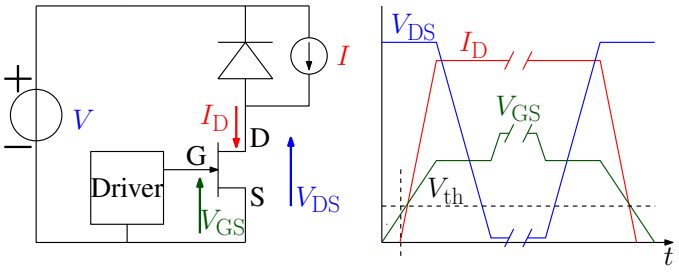


Fig. 1: Power transistor switching mesh and ideal switching waveforms

TABLE I: Basic technical data of "Normally-off" SiC-JFET (SJEP120R063)

Nominal voltage	1200 V
Nominal current	40 A ($T_{\rm j}$ = 100°C)
Maximal junction temperature ($T_{\rm j}$)	150°C
Threshold voltage	1 V ($T_{\rm j}$ = 25°C)
Packaging	TO-247

In this paper, a "Normally-off" SiC-JFET (SJEP120R063) is studied, of which some basic technical data are listed in TABLE I. As shown in its structure in Fig. 2, $C_{\rm ds}$ can be neglected when the power transistor is in OFF-state [15], so inter-electrode capacitance $C_{\rm oss}$=$C_{\rm rss}$. When this power device is in OFF-state, its inter-electrode capacitances evolution on both $V_{\rm DS}$ and $V_{\rm GS}$ voltages have been studied by authors in [11]. In this paper, their evolution when the power transistor is in linear region will be presented, with the purpose to accurately express the power transistor switching behaviors.

In this paper, firstly, inter-electrode capacitance $C_{\rm gd}$ in linear region is characterized by multiple-current-probe (MCP) method. The obtained results are validated by comparing with another measurement using an impedance analyzer. Afterwards, the output capacitance $C_{\rm oss}$ is characterized by MCP method. Different from the OFF-state where $C_{\rm oss}$ values equal to $C_{\rm rss}$ values (confirming the absence of $C_{\rm ds}$ for this transistor), a huge increase of its apparent values is observed in linear region. This result is further verified by a second measurement based on single-pulse characterization. The power transistor internal gate resistance $R_{\rm g}$ is then taken into consideration during the characterization. Its influence on obtained results by both MCP and single-pulse method will be detailed. Afterwards, a SiC-JFET behavioral model based on these characterization results is proposed, of which the switching waveforms are compared with the experimental

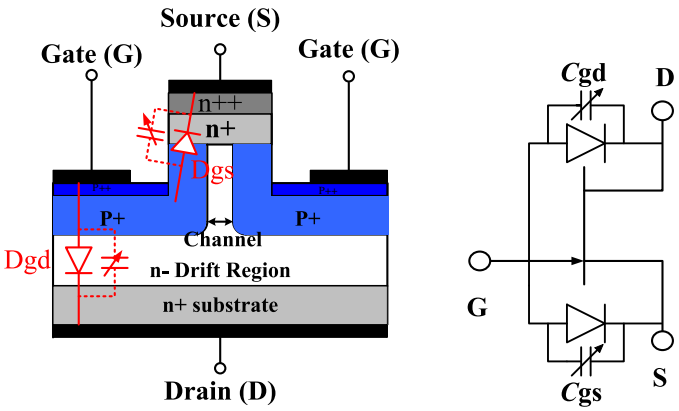


Fig. 2: "Normally-off" SiC-JFET structure and equivalent circuit

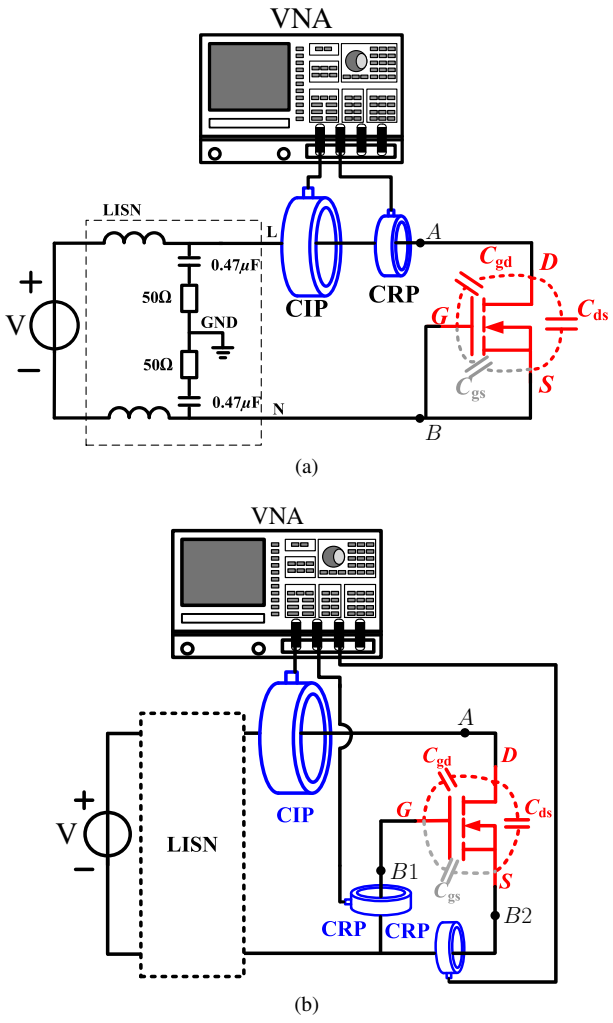


Fig. 3: Power transistor inter-electrode capacitance measurement by MCP method. (a) Using two current probes; (b) Using three current probes

results. The paper is terminated by a conclusion which presents the principle results.

II. Inter-electrode Capacitances Measurement by MCP Method

In this section, the MCP method used to measure inter-electrode capacitances of a power transistor in OFF-state is reviewed. Then, an improved measurement circuit by using this method to measure inter-electrode capacitances of a power transistor in ON-state is proposed.

A. Transistor in OFF-state

The MCP method, which is based on the use of a vector network analyzer (VNA) and several current probes, has been reported by authors in [16] to measure inter-electrode capacitances of a power transistor in OFF-state. Depending on the number of current probes, MCP method can be divided on two-current-probe method (one current injection probe (CIP), one current receiving probe (CRP), see Fig. 3a) and three-current-probe method (one CIP, two CRPs, see Fig. 3b).

The principle of the MCP method is that the VNA injects an AC current in the measurement circuit through the CIP, and when this current passes through an unknown impedance, it is measured by a CRP. Unknown impedance can be finally obtained by knowing the relation between the voltage of each port of the VNA, which is defined in the form of S-parameter, during the measurement.

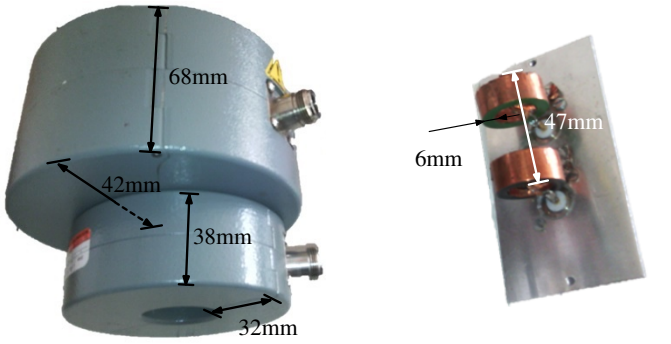
For the measurement circuit shown in Fig. 3a, the injected current flows through the parallel association of both inter-electrode capacitances $C_{\rm gd}$ and $C_{\rm ds}$. Thus, the measured impedance $Z_{\rm meas}$ at one measurement equals to:

$$\underline{Z_{\rm meas}} = \underline{Z_{\rm setup}} + \underline{Z_{\rm x}} \qquad (1)$$

where $Z_{\rm setup}$ represents the total impedance of the measurement circuit (e.g. current probe insertion impedance, connecting wires parasitic impedance and LISN 100 Ω impedance), of which the value can be determined by preliminary measurements. In two-current-probe method, as shown in Fig.3a, $Z_{\rm setup}$ can be obtained by connecting two different precision standard resistors between point A and B to replace the power transistor. Contrary to that, in three-current-probe method shown in Fig.3b, $Z_{\rm setup}$ can be obtained by replacing the power transistor with two precision standard resistors connecting A to B1 and A to B2 separately. Then it is necessary to repeat the aforementioned step twice and in each step, two precision standard resistors of different values can be used [16]. Once its value is determined, the unknown impedance $Z_{\rm x}$ can be obtained. In this case, $Z_{\rm x}$ is the impedance of the output capacitance $C_{\rm oss} = C_{\rm ds} + C_{\rm gd}$. Thus, the $C_{\rm oss}$ evolution on different $V_{\rm DS}$ voltages can be determined in this measurement when the power transistor is in OFF-state.

Likewise, for the measurement circuit shown in Fig. 3b, the injected current flowing through $C_{\rm gd}$ is measured by one CRP and that flowing through $C_{\rm ds}$ is measured by another CRP. After determining $Z_{\rm setup}$ value by preliminary measurement, both $C_{\rm gd}$ and $C_{\rm ds}$ evolution on different $V_{\rm DS}$ voltages can be obtained in this case.

As shown in Fig. 3, $V_{\rm GS}$ is zero volt, but it could also be polarized negatively by a battery. The results of a SiC JFET inter-electrode capacitance evolution for different $V_{\rm DS}$ and $V_{\rm GS}$ voltages can be found in [11] when the transistor is



Commercial current probes Realized current probes

Fig. 4: Commercialized current probes and those used in the paper

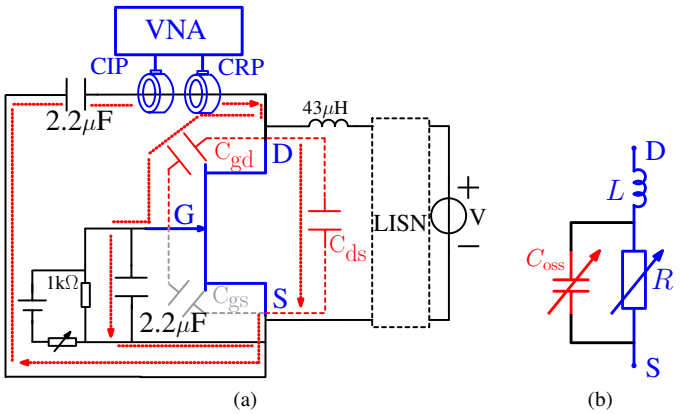


Fig. 5: (a) $C_{\rm oss}$ measurement configuration and (b) small-signal equivalent circuit by the MCP method

in OFF state.

B. Extension to transistor in ON-state

As shown in eq.(1), $Z_{\rm x}$ is obtained by a subtraction. When the power transistor is in OFF-state, $Z_{\rm x}$ value is much bigger than $Z_{\rm setup}$ value around 1MHz, which corresponds to the frequency in which the inter-electrode capacitance values are determined. However, when the power transistor is in ON-state, $Z_{\rm x}$ value can be smaller than $Z_{\rm setup}$ value because of the channel conduction. In order to avoid measurement error by subtracting two big values to get a small one, it is necessary to decrease $Z_{\rm setup}$ value.

For this reason, at first, current probes used in this paper are those developed in the laboratory [17]. It is shown in Fig. 4 the comparison between the commercialized current probes and those used in this paper. The use of those small current probes can help to decrease the measurement loop dimension, thus decrease the current probes insertion impedance in the circuit as well as the connecting wire parasitic impedance. Thus, measurement sensibility can be increased. However, those smaller current probes are easily saturated by DC current. This drawback makes the measurement configuration in Fig. 3a inapplicable to ON-state characterization where the channel may conduct high DC current.

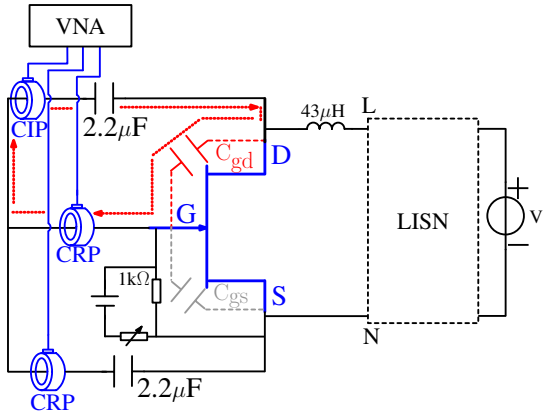


Fig. 6: $C_{\rm gd}$ measurement configuration when power transistor is in ON-state

For this reason, a new measurement circuit to characterize $C_{\rm oss}$ value is proposed in Fig. 5a. In this test configuration, a first 2.2μF capacitor is used to block the DC voltage between D and S in order to avoid the saturation of those smaller current probes by DC current. Meanwhile, a second capacitor of the same value is connected between G and S, in order to make G and S in short circuit around 1 MHz, because its impedance at this frequency is much smaller than that of $C_{\rm gs}$. A high impedance circuit is constituted by a 43μH inductor together with the LISN to guarantee that all the injected AC current flows through the power transistor.

In Fig. 5a, $Z_{\rm setup}$ is constituted by smaller current probe insertion impedance, connection wire parasitic impedance in the measurement loop and the impedance of the 2.2μF capacitor, which is much smaller than the $Z_{\rm setup}$ value in the measurement configuration shown in Fig. 3a.

An equivalent circuit of the power transistor in this characterization is represented in Fig. 5b, where R represents dynamic resistance value of the channel, L represents bonding wire parasitic inductance inside the power transistor packaging. Thus, $C_{\rm oss}$ evolution when the power transistor is in ON-state can be obtained in this measurement configuration.

Similar to the above explanations, the three-current-probe method presented in Fig. 3b is not applicable to characterize the device capacitances when the channel is in conduction. For this reason, another measurement configuration is proposed in Fig. 6 to measure $C_{\rm gd}$ value when power transistor is in ON-state. Two external 2.2μF capacitors are used to block the DC voltage between D and G, and between G and S in order to avoid the saturation of those smaller current probes by DC current. In the current loop represented by the red dotted line in Fig. 6, part of the injected current by CIP passes through $C_{\rm gd}$ and is then measured by the CRP, so $C_{\rm gd}$ values can be measured directly. The next section will present the result of such ON-state characterizations.

III. SiC-JFET Inter-electrode Capacitances Characterization

A. $C_{\rm gd}$ characterization

1) Multiple-current-probe (MCP) method: When the SiC-JFET is in linear region, $C_{\rm gd}$ is first characterized by MCP

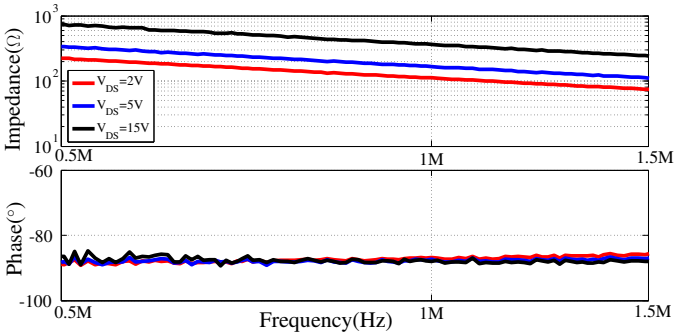


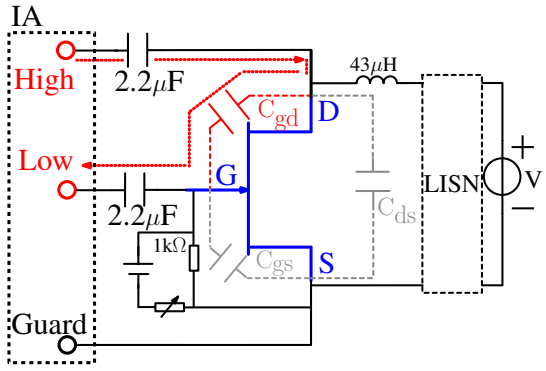
Fig. 7: C_{gd} measurement results for different V_{DS} values ($V_{\mathrm{GS}} = 1.4V$) by MCP method

method, of which the measurement circuit is illustrated in Fig. 6. In the measurement, junction temperature T_{j} is controlled to be constant at 25°C by using the relation $T_{\mathrm{j}} = T_{\mathrm{m}} + R_{\mathrm{th(tot)}}P$, where T_{m} is the measured temperature, $R_{\mathrm{th(tot)}}$ is the total thermal resistance between the power transistor junction to the measurement point (including the device junction-case thermal resistance, case-sink thermal resistance and the isolation material thermal resistance between the device and the heat sink) and P is power transistor dissipated power. When P increases, it is necessary to decrease T_{m} in order to maintain T_{j} constant, which is realized by controlling the rotation speed of a fan in the measurement.

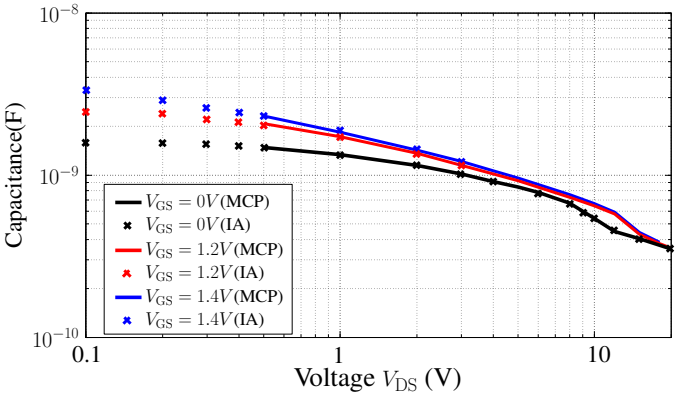
When $V_{\mathrm{GS}} = 1.4$V, the measured C_{gd} impedance and phase at different V_{DS} voltages is shown in Fig. 7. It can be seen that the measured phase is almost -90° around 1MHz, which indeed corresponds to a capacitance behavior. Thus, C_{gd} values can be obtained directly.

2) Measurement by an impedance analyzer: To validate the above C_{gd} measurement results by the MCP method, another measurement based on impedance analyzer (IA) (HP4294A, 40Hz-110MHz) is presented in Fig. 8a. The measurement principle is similar to that presented in the above section. The use of the Guard of the IA guarantees that the injected AC current flowing through C_{ds} flows directly to the Guard (the potential of Guard is the same as Low) [18]. C_{gd} evolution is thereby directly measured, which is illustrated by the red dotted line showing in the current flow in Fig. 8a. Its values are also obtained around 1MHz.

When V_{GS} is $1.2V$ and $1.4V$, C_{gd} characterization results of the above two methods are compared in Fig. 8b, in which it is shown that C_{gd} measured by the MCP method corresponds perfectly with that measured by IA for the small V_{DS} voltage values. This result is able to validate the presented MCP method to characterize C_{gd} values when the power device is in linear region. With the advantage such as galvanic isolation between the measurement equipment and the power source, the MCP method is well adapted to characterize C_{gd} values when the power device is in linear region. As what is shown in Fig. 8b, when the power device is in the linear region, C_{gd} increases with the increase of the V_{GS} voltage value. This result, which is involved in the power transistor switching trajectory, is important to model power device switching.



(a)



(b)

Fig. 8: C_{gd} measurement (a) configuration and (b) results at different V_{DS} and V_{GS} voltages

B. C_{oss} characterization

1) Multiple-current-probe method: C_{oss} capacitance is first characterized by the MCP method with the measurement circuit shown in Fig. 5a, where G and S are in short-circuit by an external 2.2μF capacitor. In the power transistor equivalent circuit shown in Fig. 5b, the impedance of the 2.2μF capacitor between G and S, which includes its parasitic bonding wire inductance L, can be neglected in comparison with measured C_{gd} impedance when the measurement frequency is inferior to 10MHz. Therefore, the measured admittance can be expressed by the following equation:

$$\underline{Y_{\mathrm{mes}}} = \frac{1}{R} + j\omega(C_{\mathrm{oss}}) \tag{2}$$

According to the eq.(2), output capacitance (C_{oss}) values can be finally determined by calculating the imaginary part of the measured admittance.

It is presented in Fig. 9a the measured C_{oss} admittance and phase when $V_{\mathrm{GS}} = 1.4V$ and $T_{\mathrm{j}} = 25°C$. From those measurement curves, C_{oss} values can be determined around 1MHz and they are shown in Fig. 9b.

According to the internal structure of the power device presented in Fig. 2, C_{ds} capacitance can be neglected. However, with the measurement results shown in Fig. 9b, it is shown that C_{oss} values seem to increase above 10 nanofarads when the power device is in linear region. It is surmised by this result that there is a surge increase of the C_{ds} values. In order

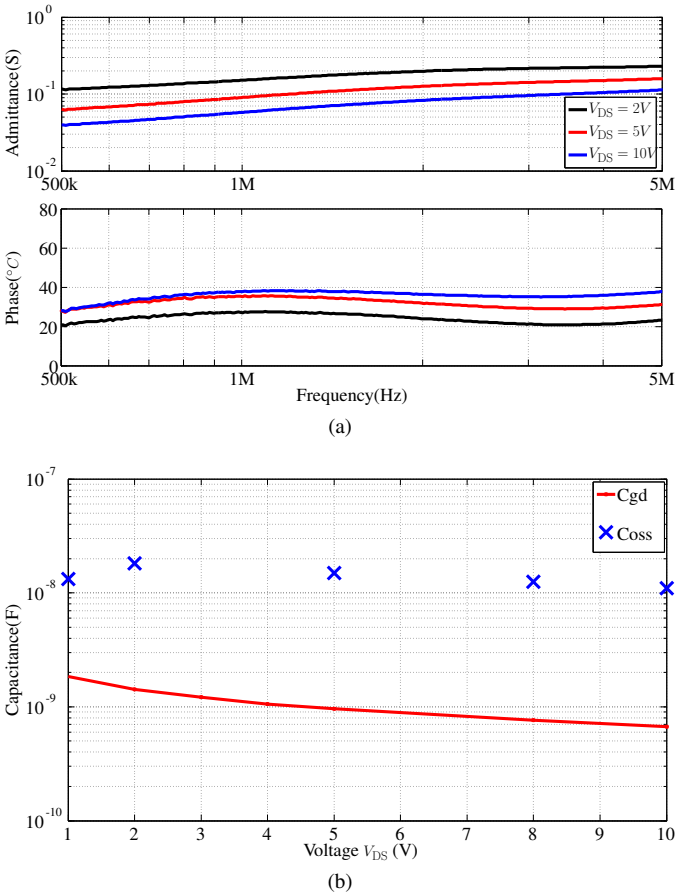


Fig. 9: (a) C_{oss} measurement results and (b) values (V_{GS}=1.4V)

to validate this result, the same power device is characterized by another measurement based on single-pulse switching.

2) single-pulse characterization: The setup of the single-pulse study is presented in Fig. 10a, which is constituted mainly from a buck converter. The device under test (DUT) is connected in series with the inductor as the load. The pulse duration t is regulated to keep T_j constant during the measurement. Current I_D is measured by an active current probe CP030 (DC-50MHz) while the voltage V_{DS} is measured by an active differential probe ADP305 (DC-100MHz). A 12-bit (600MHz) oscilloscope is used to have more precision.

It is presented in Fig. 10b the waveforms of the current I_D and the voltage V_{DS} when t is 50μs. They are then combined and presented in Fig. 10c in the form of I_D-V_{DS} plane. It is shown in Fig. 10c that at one V_{DS} voltage, the measured I_D during the pulse-ON is different from that measured during the pulse-OFF. This current difference is supposed due to the charge and discharge of C_{oss} capacitances at pulse-ON and pulse-OFF.

To verify this hypothesis, C_{oss} capacitance values are then calculated according to the RC equivalent circuit shown in Fig. 11a. The current I_D slew rate during the measurement shown in Fig. 10b is smaller than 1A/μs, so the bonding wires inductance L inside the power device packaging can be neglected. In Fig. 11a, R_s represents static resistance values of

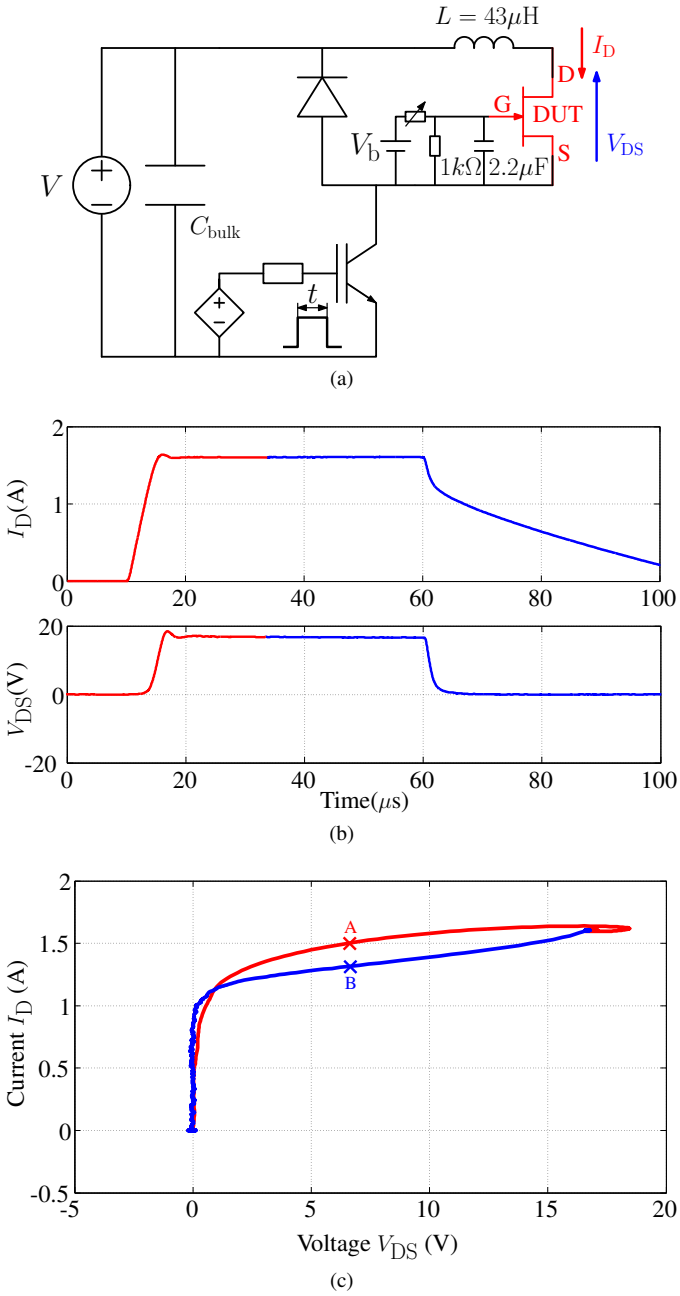


Fig. 10: Single-pulse characterization. (a) Setup; (b) Waveforms and (c) V_{DS}-I_D relation (V_{GS}=1.4V)

the SiC-JFET channel. Points A and B in Fig. 10c represent one V_{DS} value at two different instants, thus the following equation can be applied to calculate C_{oss} values.

$$\frac{V_{DS}}{R_s} = I - C_{oss} \times \left(\frac{dV_{DS}}{dt}\right) \quad (3)$$

Eq.(3) can be applied when voltage V_{DS} rises and falls, which corresponds to points A and B in Fig. 10c. Then, by varying V_{DS} voltage values in the equation, C_{oss} evolution with V_{DS} voltages can be determined when the power transistor is in linear region.

It is presented in Fig. 11b the comparison of C_{oss} values between this calculation and the measurement by the MCP

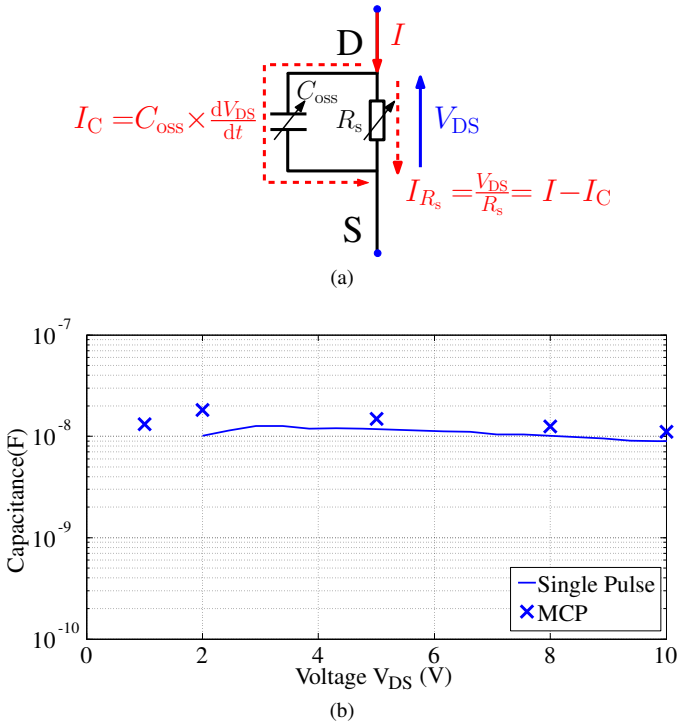


Fig. 11: (a) Equivalent circuit and (b) C_{oss} measurement results

method. It is shown that the obtained C_{oss} values by these two methods are similar, which confirms the apparent increase of C_{oss} values when the power device is in linear region.

Finally, by using the obtained R_s and C values, the equivalent circuit shown in Fig. 11a is simulated in PSpice in order to validate V_{DS} rising and falling dynamic effect. It is presented in Fig. 12 the comparison between the measurement and the simulation results, which shows a good consistency. It is surmised by this result that at one V_{GS} voltage, the power transistor can be represented by a RC circuit model shown in Fig. 11a. It can be noted that, compared to the MCP method, this calculation method based on the single-pulse measurement makes it possible to control T_j more easily due to the short self-heating duration and to determine C_{oss} values on high V_{DS} voltage values when the power device is in linear region.

The above SiC-JFET inter-electrode capacitances characterization results reveal that, when the power device is in linear region, C_{gd} capacitance increases slightly with V_{GS} voltage and C_{oss} capacitance seems to increase from around $1nF$ to more than 10 nF. Furthermore, it is presented by authors in [19] that the channel current might increase C_{ds} capacitance values by a factor of 10 for a Si-MOSFET. Thus, it may seem consistent that for this SiC-JFET, the increase of the measured C_{oss} apparent values is similarly due to a surge increase of the C_{ds} capacitance values.

However, it is observed that there is a non-neglected internal gate resistor R_g inside the power device packaging in the technical datasheet of the SiC-JFET. According to authors [20], the origin of one part of the R_g is due to the gate electrode. The influence of the R_g on characterization results is presented in the next section.

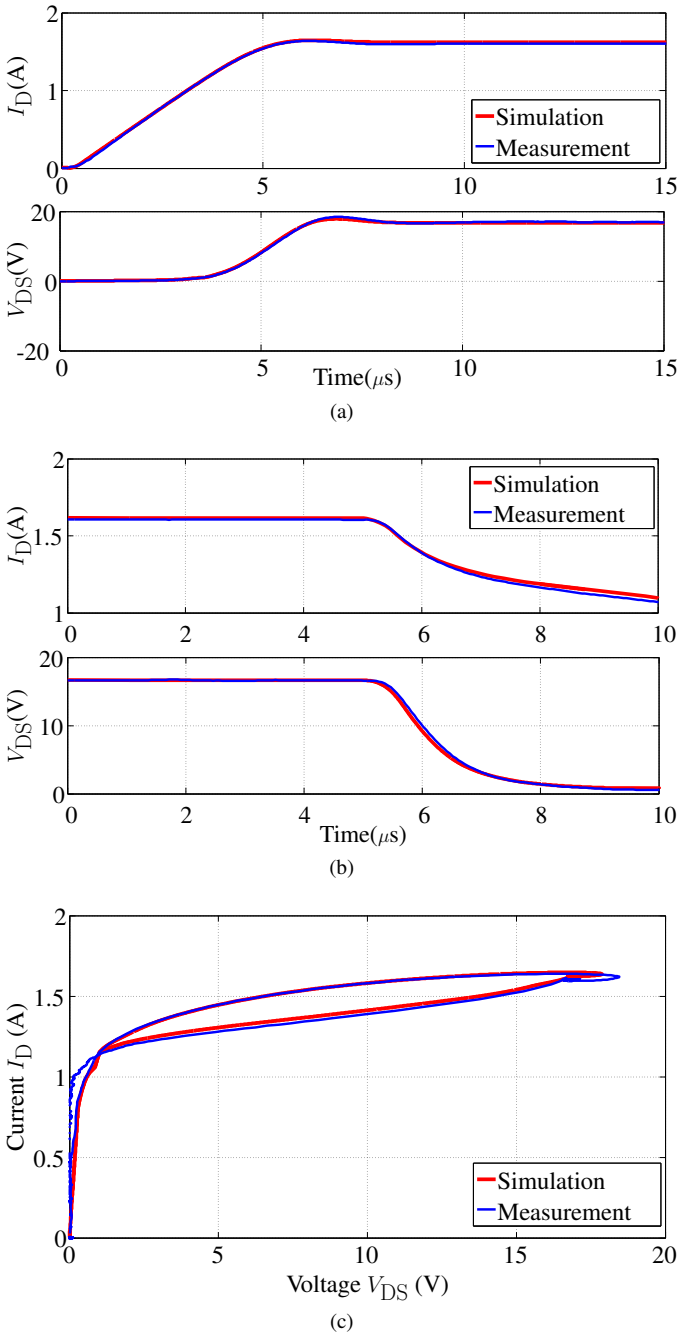


Fig. 12: Comparison between the simulation and the measurement waveforms when V_{GS}=1.4V. (a) V_{DS} rising; (b) V_{DS} falling; (c) V_{DS}-I_D

IV. Internal Gate Resistance R_g Influence

In order to present the influence of R_g on SiC-JFET characterization results when the power device is in linear region, it is necessary to model the characterization circuit with a detailed power device model. Therefore, internal gate resistor R_g and parasitic resistor of drain R_d and that of source R_s are included in the power device model in order to obtain an analytical expression of the measured impedance.

A. SiC-JFET characterization with internal R_g

1) Multiple-current-probe method characterization circuit modeling: It is presented in Fig. 13 the small-signal model to represent power device (with C_{ds} and internal parasitic resistances) inter-electrode capacitances characterization by the MCP method when the power device is in linear region. The power device physical accessible electrodes are G', D' and S'. The influence of the parasitic inductances inside the packaging on measurement results can be neglected when the measurement frequency is inferior to 10MHz. The bias voltages of V_{GS} and V_{DS} are DC voltages, so they are not represented in the circuit. The AC signal is represented by a voltage generator $\underline{V_1}$. The gate voltage $\underline{V_{GS}}$ variation can induce a channel current $\underline{I_{ch}} = g \cdot \underline{V_{GS}}$, where g represents the power transistor dynamic transconductance. When power transistor is in linear region, g is supposed to be independent of V_{DS} voltage.

For C_{gd} characterization presented in section III-A, the imaginary part of the measured impedance $Z_{C_{gd}}$, which can be expressed by $Im(\frac{V_1}{I_G})$, is calculated.

From the circuit shown in Fig. 13, the following six equations can be obtained:

$$\underline{V_{DS}} = \underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_S} \cdot R_s \tag{4}$$

$$\underline{V_{DG}} = \underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_G} \cdot R_g \tag{5}$$

$$\underline{V_{GS}} = \underline{I_G} \cdot R_g - \underline{I_S} \cdot R_s \tag{6}$$

$$\underline{I_D} = \underline{I_S} + \underline{I_G} \tag{7}$$

$$\underline{I_G} = \frac{\underline{V_{DG}}}{\underline{Z_{C_{gd}}}} - \frac{\underline{V_{GS}}}{\underline{Z_{C_{gs}}}} \tag{8}$$

$$\underline{I_D} = \frac{\underline{V_{DG}}}{\underline{Z_{C_{gd}}}} + g \cdot \underline{V_{GS}} + \frac{\underline{V_{DS}}}{\underline{Z_{C_{ds}}}} \tag{9}$$

By replacing the equations (5) (6) (7) into (8), following equations can be obtained:

$$\underline{I_G} = \frac{\underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_G} \cdot R_g}{\underline{Z_{C_{gd}}}} - \frac{\underline{I_G} \cdot R_g - \underline{I_S} \cdot R_s}{\underline{Z_{C_{gs}}}} \tag{10}$$

$$\underline{I_G} = \frac{\underline{V_1}}{\underline{Z_{C_{gd}}}} - \left(\frac{R_g}{\underline{Z_{C_{gd}}}} + \frac{R_g}{\underline{Z_{C_{gs}}}} + \frac{R_s}{\underline{Z_{C_{gs}}}} \right) \cdot \underline{I_G} + \left(\frac{R_s}{\underline{Z_{C_{gs}}}} - \frac{R_d}{\underline{Z_{C_{gd}}}} \right) \cdot \underline{I_D} \tag{11}$$

Similarly, by replacing the equations (4) (5) (6) (7) into (9), following equation is obtained:

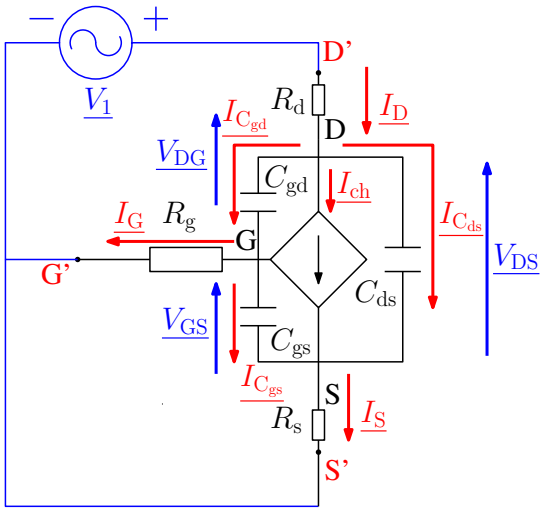


Fig. 13: Small-signal model of the characterization circuit by the MCP method when power transistor in linear region

$$\underline{I_D} = \frac{\underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_G} \cdot R_g}{\underline{Z_{C_{gd}}}} + g \cdot \underline{I_G} \cdot R_g - g \cdot \underline{I_S} \cdot R_s + \frac{\underline{V_1} - \underline{I_D} \cdot R_d - \underline{I_S} \cdot R_s}{\underline{Z_{C_{ds}}}} \tag{12}$$

By using $s = j\omega$ in the equations (11) et (12), following equations can be obtained:

$$sC_{gd}\underline{V_1} = (1 + sC_{gd}R_g + sC_{gs}R_g + sC_{gs}R_s) \cdot \underline{I_G} - (R_s sC_{gs} - R_d sC_{gd}) \cdot \underline{I_D} \tag{13}$$

$$(sC_{gd} + sC_{ds}) \cdot \underline{V_1} = (R_g sC_{gd} - R_s sC_{ds} - gR_g - gR_s) \cdot \underline{I_G} + (1 + sC_{gd}R_d + sC_{ds}R_d + sC_{ds}R_s + gR_s) \cdot \underline{I_D} \tag{14}$$

In the SiC-JFET technical datasheet, the value of the resistor R_g may equal to several ohms, while that of R_s is inferior to several tens of milliohms. Thus, with the hypothesis $R_g \gg R_s$, the above equations (13) and (14) can be simplified into the following forms:

$$sC_{gd}\underline{V_1} = (1 + sC_{gd}R_g + sC_{gs}R_g) \cdot \underline{I_G} - (R_s sC_{gs} - R_d sC_{gd}) \cdot \underline{I_D} \tag{15}$$

$$(sC_{gd} + sC_{ds}) \cdot \underline{V_1} = (R_g sC_{gd} - R_s sC_{ds} - gR_g) \cdot \underline{I_G} + (1 + sC_{gd}R_d + sC_{ds}R_d + sC_{ds}R_s + gR_s) \cdot \underline{I_D} \tag{16}$$

Multiplying eq.(15) by $(1 + sC_{gd}R_d + sC_{ds}R_d + sC_{ds}R_s + gR_s)$ and multiplying eq.(16) by $(R_s sC_{gs} - R_d sC_{gd})$ and then adding the two equations, the current $\underline{I_D}$ can be canceled in equations (15) and (16), so the equation below is thus obtained:

$$A1 \cdot \underline{I_G} = B1 \cdot \underline{V_1} \tag{17}$$

R_d is supposed to be the same magnitude to R_s, so the following hypothesis can be validated:

$$\begin{aligned} &R_\mathrm{g} \gg R_\mathrm{s}, \quad R_\mathrm{g} \gg R_\mathrm{d}, \\ &\text{and until 10MHz} \quad 1 \gg \omega^2 C_{XY} C_{XY} R_X R_Y \end{aligned} \tag{18}$$

where X,Y are index which indicate either d, g or s.

By applying this hypothesis, A1 and B1 in eq.(17) can be expressed in the following forms:

$$A1 = 1 + gR_\mathrm{s} + s\left(C_\mathrm{gd}R_\mathrm{g} + 2C_\mathrm{ds}R_\mathrm{s} + C_\mathrm{gs}R_\mathrm{g} + 2gC_\mathrm{gd}R_\mathrm{g}R_\mathrm{s}\right) \tag{19}$$

$$B1 = -R_\mathrm{s}\omega^2\left(C_\mathrm{gd}C_\mathrm{gs} + C_\mathrm{gd}C_\mathrm{ds} + C_\mathrm{ds}C_\mathrm{gs}\right) + s\left(1 + gR_\mathrm{s}\right)C_\mathrm{gd} \tag{20}$$

For C_gd measurement, the imaginary part of the measured impedance $Im\left(\frac{V_1}{I_\mathrm{G}}\right)$ can be expressed by:

$$Im\left(\frac{\underline{V_1}}{\underline{I_\mathrm{G}}}\right) = \frac{E}{F} \tag{21}$$

where:

$$\begin{aligned} E = &-R_\mathrm{s}\omega^3\left(C_\mathrm{gd}C_\mathrm{gs} + C_\mathrm{gd}C_\mathrm{ds} + C_\mathrm{ds}C_\mathrm{gs}\right) \\ &\times\left(C_\mathrm{gd}R_\mathrm{g} + 2C_\mathrm{ds}R_\mathrm{s} + C_\mathrm{gs}R_\mathrm{g} + 2gC_\mathrm{gd}R_\mathrm{g}R_\mathrm{s}\right) \\ &-\omega\left(1 + gR_\mathrm{s}\right)^2 C_\mathrm{gd} \end{aligned} \tag{22}$$

and:

$$\begin{aligned} F = &\left(R_\mathrm{s}\omega^2\left(C_\mathrm{gd}C_\mathrm{gs} + C_\mathrm{gd}C_\mathrm{ds} + C_\mathrm{ds}C_\mathrm{gs}\right)\right)^2 \\ &+\omega^2\left(1 + gR_\mathrm{s}\right)^2 {C_\mathrm{gd}}^2 \end{aligned} \tag{23}$$

By using the same hypothesis (18), eq.(21–23) can be simplified into:

$$Im\left(\frac{\underline{V_1}}{\underline{I_\mathrm{G}}}\right) = \frac{1}{\omega C_\mathrm{gd}} \tag{24}$$

It is shown in the above equation that when the power device is in linear region, C_gd measurement in the circuits presented in Fig. 6 and Fig. 8a is valid to characterize its values. In other words, the internal resistor R_g does not interfere with the C_gd measurement.

In contrast, the determination of C_oss is not so straightforward, as will be shown below.

For the C_oss measurement presented in section III-B, the imaginary part of the measured admittance Y_{C_oss}, which can be expressed by $Im(\frac{I_\mathrm{D}}{V_1})$, is calculated.

Multiplying eq.(15) by $\left(R_\mathrm{g}sC_\mathrm{gd} - R_\mathrm{s}sC_\mathrm{ds} - gR_\mathrm{g}\right)$ and multiplying eq.(16) by $\left(1 + sC_\mathrm{gd}R_\mathrm{g} + sC_\mathrm{gs}R_\mathrm{g}\right)$ and then subtracting the two equations, the current $\underline{I_\mathrm{G}}$ in equations (15) and (16) can be canceled, the following equation can thus be obtained:

$$A2 \cdot \underline{I_\mathrm{D}} = B2 \cdot \underline{V_1} \tag{25}$$

By applying the same hypothesis (18), A2 and B2 in eq.(25) can be expressed in the following form:

$$A2 = 1 + gR_\mathrm{s} + s\left(C_\mathrm{gd}R_\mathrm{g} + 2C_\mathrm{ds}R_\mathrm{s} + C_\mathrm{gs}R_\mathrm{g} + 2gC_\mathrm{gd}R_\mathrm{g}R_\mathrm{s}\right) \tag{26}$$

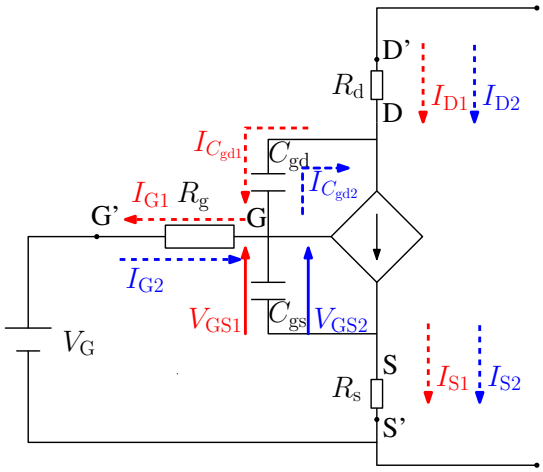


Fig. 14: SiC-JFET characterization by single-pulse method with R_g, R_d and R_s

$$\begin{aligned} B2 = &-R_\mathrm{g}\omega^2\left(C_\mathrm{gd}C_\mathrm{gs} + C_\mathrm{gd}C_\mathrm{ds} + C_\mathrm{ds}C_\mathrm{gs}\right) \\ &+s\left(C_\mathrm{ds} + C_\mathrm{gd} + gC_\mathrm{gd}R_\mathrm{g}\right) \end{aligned} \tag{27}$$

For C_oss measurement, by using the same hypothesis (18), the imaginary part of the measured admittance $Im\left(\frac{I_\mathrm{D}}{V_1}\right)$ can be expressed in the following relation:

$$Im\left(\frac{\underline{I_\mathrm{D}}}{\underline{V_1}}\right) = \omega\frac{C_\mathrm{ds} + C_\mathrm{gd} + gR_\mathrm{g}C_\mathrm{gd}}{1 + gR_\mathrm{s}} \tag{28}$$

Unlike C_gd measurement, it is shown in the above relation that when the power device is in linear region, the measured C_oss values by the circuit shown in Fig. 5a no longer equals to $C_\mathrm{oss} = C_\mathrm{ds} + C_\mathrm{gd}$. In fact, power transistor dynamic transconductance g and its internal gate resistance R_g will increase the apparent capacitance values by a term $g \cdot R_\mathrm{g} \cdot C_\mathrm{gd}$, which reveals the influence of the internal gate resistance on measurement results.

2) single-pulse characterization circuit modeling: It is presented in section III-B that the difference of the current I_D values at one V_DS voltage (Fig. 10c) is possibly due to the charge and discharge of the C_oss capacitance at pulse-ON and pulse-OFF. It is presented in Fig. 14 the SiC-JFET characterization circuit by single-pulse method, in which R_g, R_d and R_s are included in the power device model. It is illustrated by red lines the direction of each electrical variable during the pulse-ON, which corresponds to $\mathrm{d}V_\mathrm{DS}/\mathrm{d}t > 0$ with the indicated trajectory in Fig. 10c. It is illustrated by blue lines the direction of each electrical variable during the pulse-OFF, which corresponds to $\mathrm{d}V_\mathrm{DS}/\mathrm{d}t < 0$ with the indicated trajectory in Fig. 10c.

It is shown in Fig. 14 that during pulse-ON, C_gd charge current I_{C_gd} passes through R_g, which induces a drop voltage V_{R_g} across R_g; also the source current I_S passes through R_s, which induces a voltage V_{R_s} across R_s. Thus, during the pulse-ON, the voltage V_GS1 can be calculated by the following equation:

$$V_\mathrm{GS1} = V_\mathrm{G} + I_\mathrm{G1}R_\mathrm{g} - I_\mathrm{S1}R_\mathrm{s} \tag{29}$$

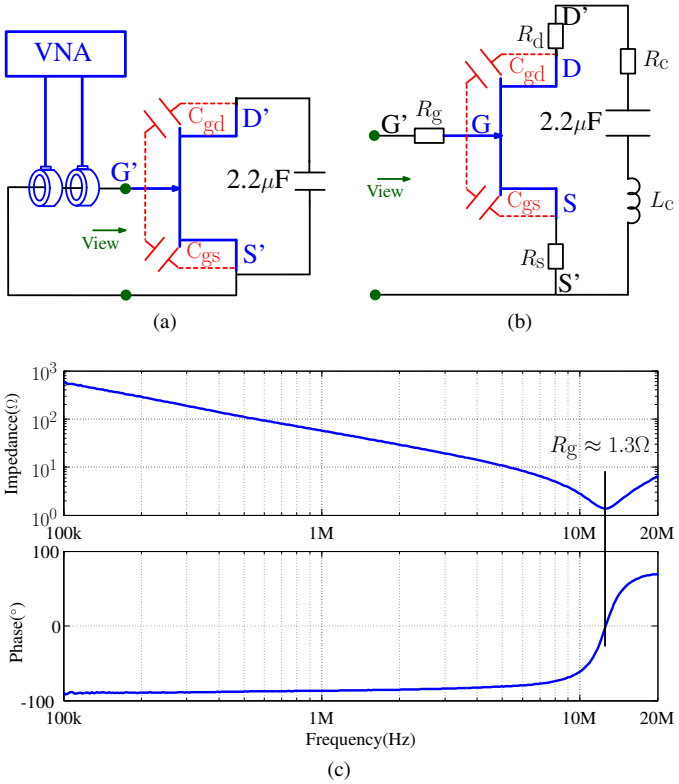


Fig. 15: Determination of R_g value. (a) Measurement circuit; (b) Equivalent circuit when SiC-JFET is blocked; (c) Measurement result

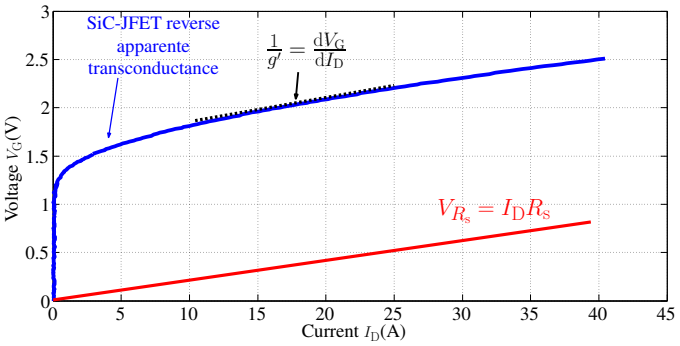


Fig. 16: The method to estimate R_s resistance

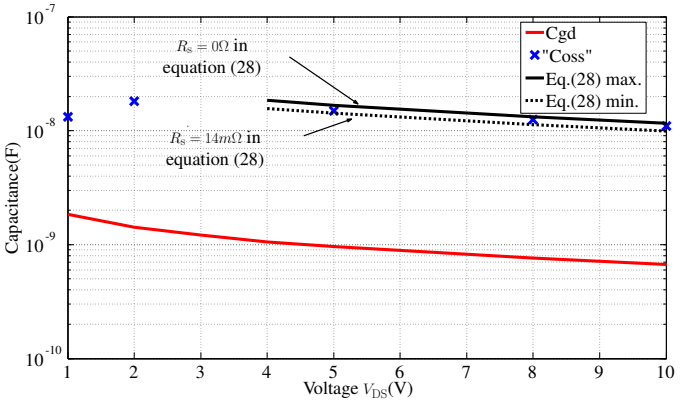


Fig. 17: Apparent "Coss" capacitance measurement results when the SiC-JFET in linear region ($V_{GS} = 1.4$V)

The similar analysis can be applied in pulse-OFF process, thus during the pulse-OFF, the voltage V_{GS2} can be calculated by:

$$V_{GS2} = V_G - I_{G2}R_g - I_{S2}R_s \tag{30}$$

It is shown in the equations (29) and (30) that because of the R_g and R_s resistances, V_{GS} is no longer the imposed voltage V_G during the characterization. By applying the measurement data in Fig. 10c, it can be verified that $V_{GS1} > V_{GS2}$ during the characterization. Thus, the difference of the drain current in Fig. 10c is partly due to this V_{GS} voltage difference and not due to a surge increase of C_{ds} capacitance values.

It is shown in this part and the previous one that both R_g and R_s resistances have influence on the obtained capacitance values, thus it is necessary to estimate their values, which will be presented in the next part.

3) Internal resistances R_g and R_s estimation: The R_g resistance can be estimated with the measurement circuit shown in Fig. 15a using the MCP method [16]. When the SiC JFET is blocked, it can be represented by the equivalent circuit shown in Fig. 15b, in which the 2.2μF external capacitor is modeled by its capacitance in series with the equivalent series resistance (ESR) R_c and the equivalent series inductance (ESL) L_c. As R_g is the biggest resistance and it is much bigger than R_s, its value is obtained from the results shown in Fig. 15c, in which it is given by the resonance frequency. Thus, its value can be estimated about 1.3Ω.

There is also a term $1 + gR_s$ in the denominator of the eq.(28), so it is necessary to estimate R_s value to quantify its influence on the measurement results. For this reason, its superior boundary is calculated by the following method. First, according to the power device model presented in Fig. 14, the obtained I_D-V_G curve in the measurement is an apparent transconductance, in which V_G is altered by the term $I_D \cdot R_s$ that is illustrated in Fig. 16.

Nevertheless, as shown in Fig. 16, R_s can not be superior to reverse apparent dynamic transconductance: $\frac{1}{g'} = \frac{dV_G}{dI_D}$. Otherwise, the real power device dynamic transconductance $g = \frac{dI_D}{dV_{GS}}$ obtained from:

$$\frac{1}{g} = \frac{dV_{GS}}{dI_D} = \frac{dV_G}{dI_D} - R_s = \frac{1}{g'} - R_s, \tag{31}$$

would be inferior to 0, which means an impossible negative dynamic transconductance is obtained. Therefore, it is necessary that R_s is inferior to $\left(\frac{dV_G}{dI_D}\right)_{min}$, which is about 14 milliohms in this case. As a consequence, it can be stated that $R_g >> R_s$.

The estimated R_g and R_s values are used in the following paragraphs to validate the characterization results.

B. Validation

The characterization results, by the MCP and single-pulse methods, are validated by including the influence of the SiC-JFET internal R_g.

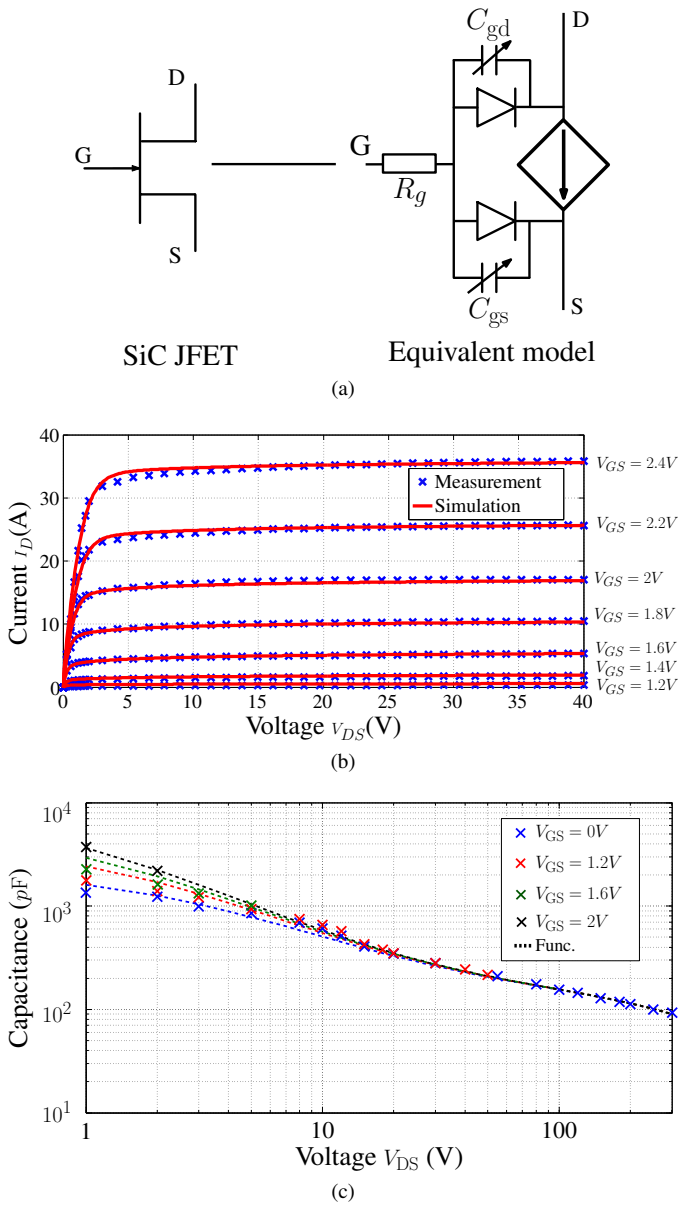


Fig. 18: Comparison between the model and the measurement of SiC-JFET characteristics ($T_j = 25°C$). (a) SiC-JFET model; (b) Static characteristics, (c) C_{gd} capacitance values

1) Multiple-current-probe method characterization: As what is shown in eq.(24), C_{gd} capacitance measurement results are not influenced by the R_g resistance when the SiC-JFET is in linear region.

With the measured C_{gd} capacitance values, the apparent "Coss" capacitance values can be calculated according to the eq.(28) and then compared to the measurement. The R_s value in eq.(28) can be varied from its minimal value 0Ω to its estimated maximal value $14m\Omega$ in section IV-A3, by which the calculation result of eq.(28) can reach its maximal value and minimal value correspondingly. Because of the SiC-JFET internal structure, $C_{ds} = 0$ is imposed in eq.(28). The calculation results are compared with the measured apparent "Coss" capacitance values in Fig. 17.

It is shown in Fig. 17 that the measured apparent "Coss" capacitance values are between the minimal and maximal calculation result of the eq. (28). Therefore, when the power device is in linear region, the surge increase of the "Coss" capacitance values is certainly due to the influence of gR_g on the measurement and not due to an increase of the C_{ds} capacitance values.

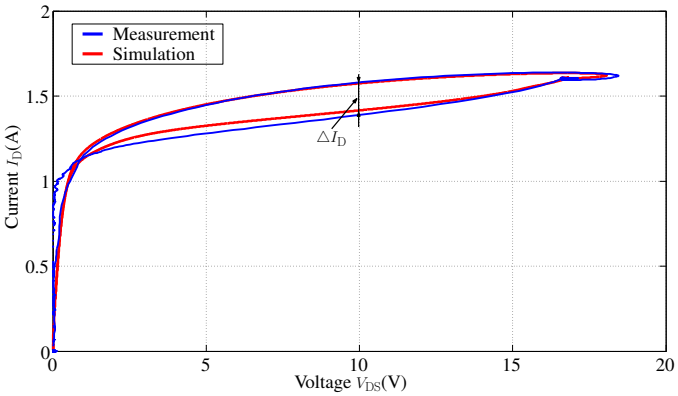


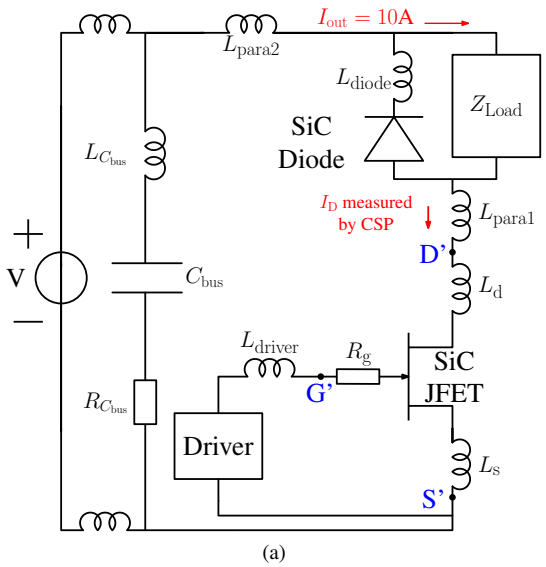
Fig. 19: Comparison of I_D-V_{DS} between the model and the measurement ($V_{GS} = 1.4V$, $T_j = 25°C$)

2) single-pulse characterization: To validate the influence of R_g on the current I_D difference observed in Fig. 10c, a SiC-JFET behavioral model presented in Fig. 18a is used in the simulation circuit shown in Fig. 10a, in which the SiC-JFET is polarized with $V_{GS} = 1.4V$. The comparison between the simulation and the measurement of static characteristic has been presented in Fig. 18b. The following equation eq.(32) is used to express C_{gd} capacitance values when the SiC-JFET is in linear region with $0V \leq V_{GS} \leq 2V$. The parameters are obtained by the fitting method: $a = 8.24 \times 10^3, b = 0.7625, c = 1.12, d = 1.5 \times 10^2, e = 0.0021$ (various units to satisfy the equation where V_{GS}, V_{DS} voltages are expressed in volts and C_{rss} in picofarads). The comparison between the chosen function and the measurement is shown in Fig. 18c.

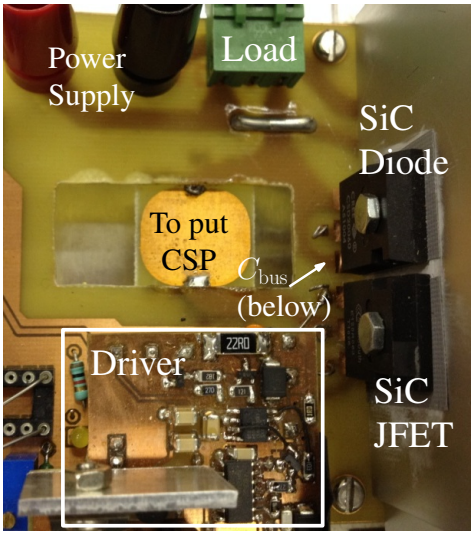
$$C_{rss} = \frac{a}{1 + \left(\frac{V_{DS} - V_{GS} + 2}{b}\right)^c} + d \cdot \exp\left(-e \cdot (V_{DS} - V_{GS} + 2)\right) \tag{32}$$

It is presented in Fig. 19 that the presented power device model reproduces almost the same current difference ΔI_D at one V_{DS} voltage during the current rising and falling. Actually, some difference can be noticed between the measurement and model depending on V_{DS} (up to about 30%). As ΔI_D directly depends on g, it is principally due to their difference on dynamic transconductance. Indeed, small differences are likely to occur between the static characterization dataset and the fitting functions, because I-V curves are first fitted for each V_{GS}, and then the obtained parameters are fitted as functions of V_{GS}. Still, it is shown in Fig. 19 that ΔI_D is principally due to the ΔV_{GS} variation during the characterization.

Thus, it is presented in the above results the influence of the R_g resistance on characterization results by both the MCP and the single-pulse methods. The results in this section reveal that the increase of the apparent C_{oss} capacitance values when the power device is in linear region is due to the internal gate



(a)



(b)

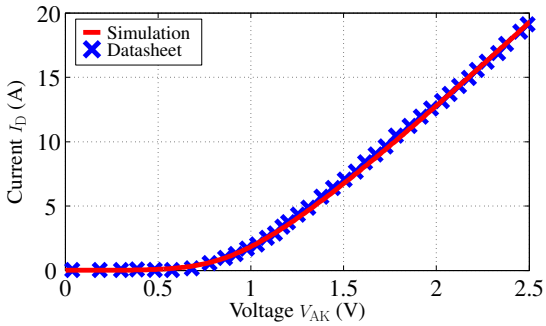
Fig. 20: SiC-JFET (a) switching circuit including parasitic inductances and (b) its realization

R_g resistance. This resistance can vary V_{GS} voltage during the characterization, thus increase the measured C_{oss} capacitance values. The SiC-JFET model when including the measured C_{gd} values variation and when considering $C_{ds} = 0$ is then compared with the measurement on switching in the next section.

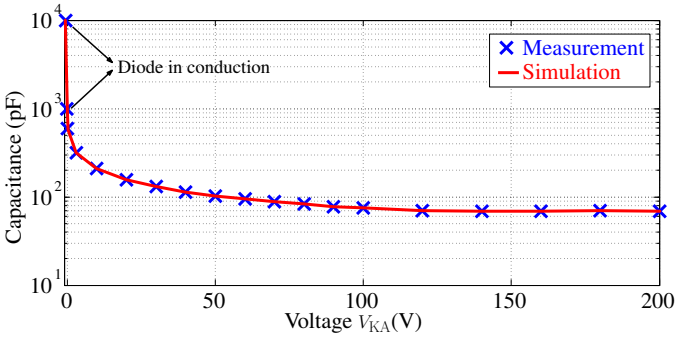
V. SiC-JFET Model Validation

A buck converter with the studied SiC-JFET and one SiC-diode (CSD20060D) in the circuit shown in Fig. 20a is used to measure switching waveforms. The transistor is controlled by a driver based on the similar circuit presented in [21]. The power converter realization is shown in Fig. 20b.

The measurement conditions are: $V = 120$V and $I_{out} = 10$A. Voltage V_{DS} is measured by a voltage passive probe (VP) PPE4kV (4kV, 400MHz), while current I_D is measured by a current surface probe (CSP) FCC F-96 (1MHz-450MHz).



(a)



(b)

Fig. 21: SiC diode modeling. (a) Static characteristic; (b) Dynamic characteristic

The transfer impedance of the CSP is obtained at first on a PCB with the same geometry to that used in the power converter. CSP transfer impedance can then be used to correct the measured current. More details on how to use the CSP are presented in [22].

The bus capacitor C_{bus} and the load are characterized with the impedance analyzer. An equivalent circuit valid until 100MHz of each component is proposed in the simulation circuit in PSpice. The parasitic inductances of the switching loop are indicated in Fig. 20a, in which the measured $L_{C_{bus}} = 4n$H, $L_{para1} = 25n$H (lumped value), $L_{para2} = 15n$H, $L_{diode} = 4n$H and $L_{driver} = 36n$H (lumped value) represent parasitic inductances in the bus capacitor, power converter, diode packaging and the driver circuit. The $L_d = 2n$H and $L_s = 6n$H represent parasitic inductances inside the power transistor packaging. The gate parasitic inductance can be neglected in comparison with L_{driver}, thus only internal gate resistor R_g with its measured value is added in the simulation circuit. The SiC-diode static characteristic is modeled by a current generator and its dynamic characteristic is modeled by its junction capacitor C_j evolution, which are shown in Fig. 21. The SiC-JFET is modeled by its equivalent circuit shown in Fig. 18a.

The switching waveforms comparison between the model and the measurement when the gate resistance of the driver $R_{driver} = 1\Omega$ is shown in Fig. 22. It is shown that turn-on and turn-off transitions are about $20n$s. The model of the SiC-JFET represents correctly both the di/dt, dv/dt during the switchings and the resonance behavior, which is mainly due to the resonance between the switching loop parasitic

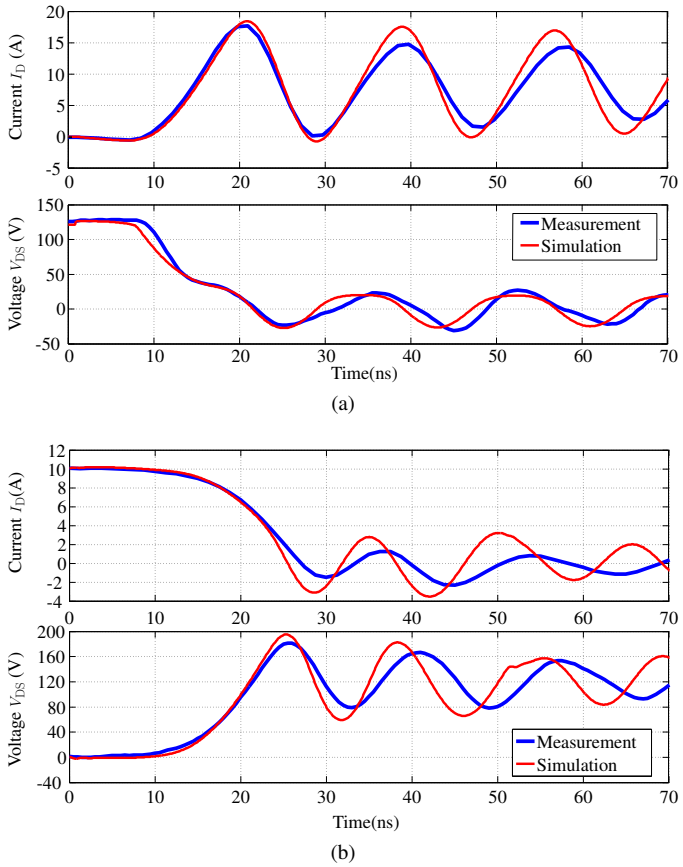


Fig. 22: Comparison between the model and the measurement when $R_{\text{driver}} = 1\Omega$. (a) Turn-on waveforms; (b) Turn-off waveforms

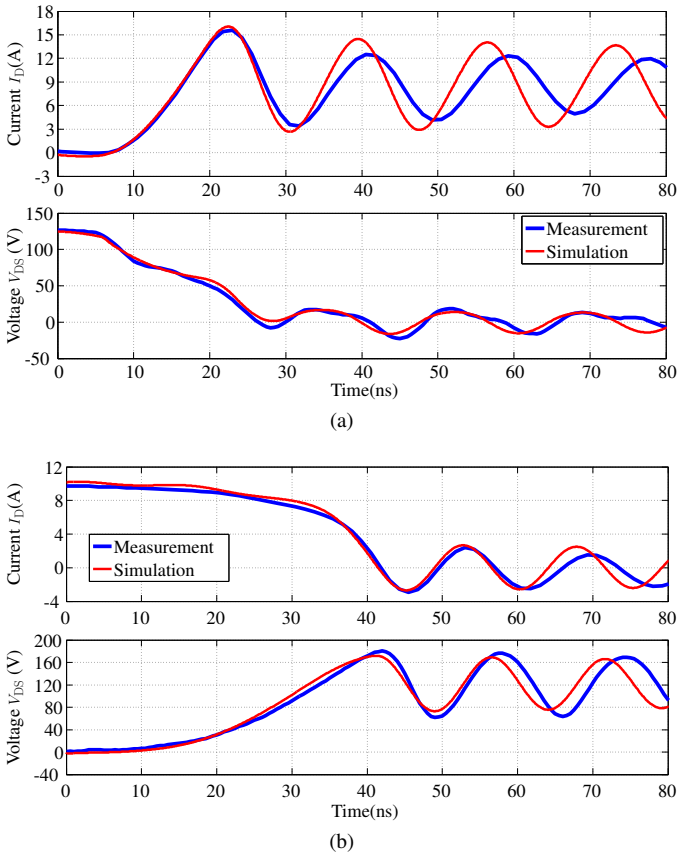


Fig. 23: Comparison between the model and the measurement when $R_{\text{driver}} = 10\Omega$. (a) Turn-on waveforms; (b) Turn-off waveforms

inductances with the diode C_j during SiC-JFET turn-on and with the transistor equivalent capacitance between D and S during SiC-JFET turn-off, at the end of the switching.

In order to study the robustness of the proposed model, the circuit is simulated in another switching condition when R_{driver} is 10Ω. The comparison of switching waveforms given in Fig. 23 show a good agreement between the measurement and the simulation. The results confirm the robustness of the proposed model. However, one reason of the mismatch between the simulation and the measurement is supposed to be the lack of the mutual inductance in the simulation circuit. The mutual inductance might be obtained according to some numerical simulation software such as InCa3D, COMSOL.

VI. Conclusion

In this paper, in order to finely model power semiconductor devices, the inter-electrode capacitances of a "normally-off" SiC-JFET are characterized when the power device is in linear region. The characterization of the C_{gd} based on the multiple-current-probe method is validated by the measurement in impedance analyzer. The determination of C_{oss} based on the same method is compared with another characterization in single-pulse. It is shown in the measurement results that when the SiC-JFET is in OFF-state, C_{oss} equals to C_{rss} value, which confirms the absence of the capacitance C_{ds}. However, when the power device is in linear region, it is shown in the C_{oss} measurement that its values can increase a tenfold.

It is shown by this study that the existence of a gate resistance (R_g) inside the SiC-JFET packaging influence the characterization results. Indeed, voltage V_{GS} during the characterization is varied by the current flowing through R_g, thus apparent inter-electrode capacitances are varied.

A transistor model based on the characterization results is proposed. The switching waveforms in the simulation are compared with the measurement. It is shown that the behavioral model can represent correctly the $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ switching waveforms.

The SiC-JFET inter-electrode capacitances characterization results are validated by the presence of this power transistor internal gate resistance R_g. The proposed methods in this paper can be applied to power semiconductor devices of different technologies. Special caution is necessary when the characterization in linear region of a power transistor in which the C_{ds} capacitance can not be neglected.

The comparison of the SiC-JFET behavioral models with and without its inter-electrode capacitances characterization when the power device is in the linear region will be reported in future work. The proposed model will be used to estimate the power loss and to study the EMI aspects induced by the power converters.

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